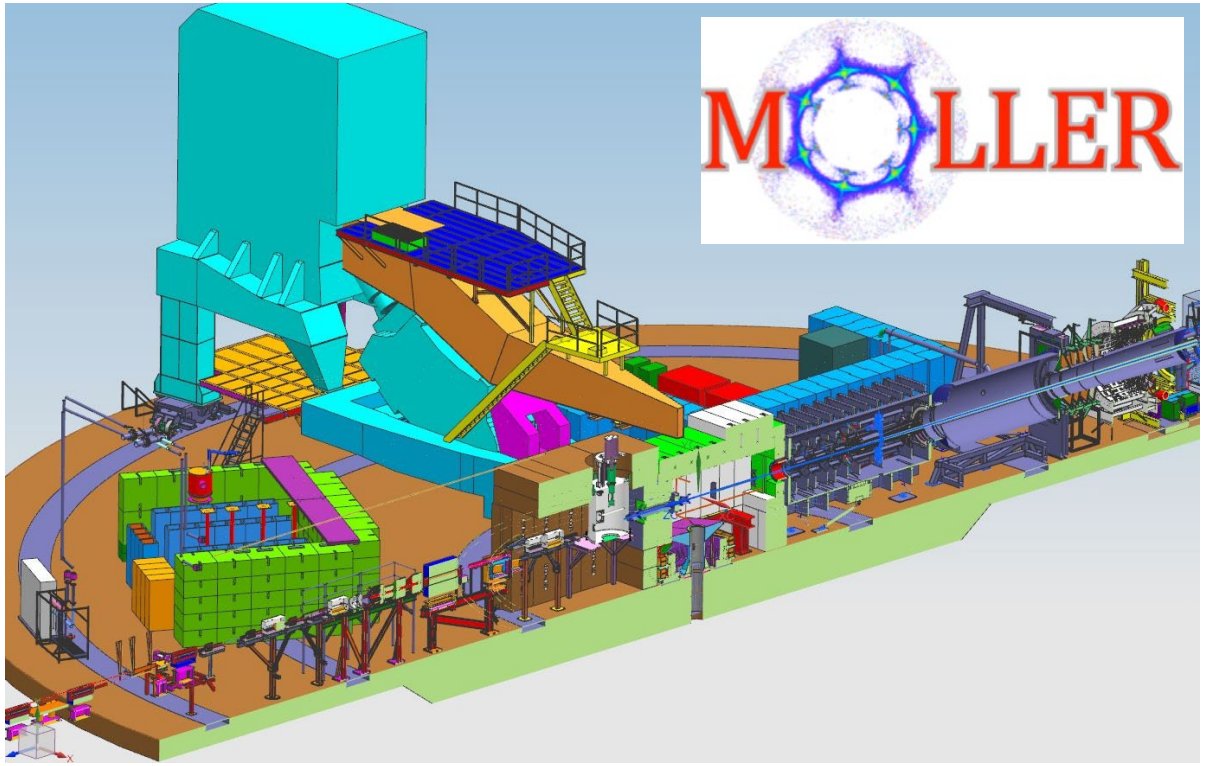
MOLLER ERR2

DAQ



Paul King, Ohio University

July 29-31, 2025

Physics needs and requirements

Integrating mode:

- Measuring A_{raw} with an uncertainty of ~0.5 ppb requires recording ~4×10^{18} e-e scatters tagged by helicity → 8256 hours at 134 GHz (65μA beam current)
  - Use detector flux integration, over periods tagged by beam helicity, to calculate flux asymmetry
  - Beam asymmetries measured simultaneously to correct the flux asymmetry
  - Helicity flipped rapidly to minimize effect of drifts in experimental conditions
  - DAQ must record all helicity periods, without deadtime
  - Feedback adjusts beam control devices to keep average beam asymmetries small

Counting mode:

- Used for checking kinematics, backgrounds, and alignment
- Extracting A_{PV} from A_{raw} requires understanding non-Moller backgrounds in the detectors
- Comparing to the SM value requires measuring the accepted Q^2 distribution
  - Measure individual particle trajectories and corresponding detector signals with very low beam currents (100pA - 100nA)
  - Allow flexible trigger definitions for input signal rates of up to 300 kHz
  - Triggers can be prescaled, and deadtime does not need to be avoided

DAQ system deliverables and KPPs

Deliverables

- Integrating DAQ
  - Integrating ADCs
  - Pre-amps
  - Point-to-point fiber links to workstations
  - VME crates, cpus, interrupt cards
  - Scalers and Input/Output
- Counting DAQ
  - Flash ADCs (JLab design)
  - Scalers, Input/Output
  - VME crates, CPUs, interrupt cards
  - GEM readout
- Computers and Disks

KPP

DAQ and trigger systems for readout of detector systems in both counting (low rate) and integrating (high rate) modes installed and stress-tested successfully

Threshold KPP and Objective KPP

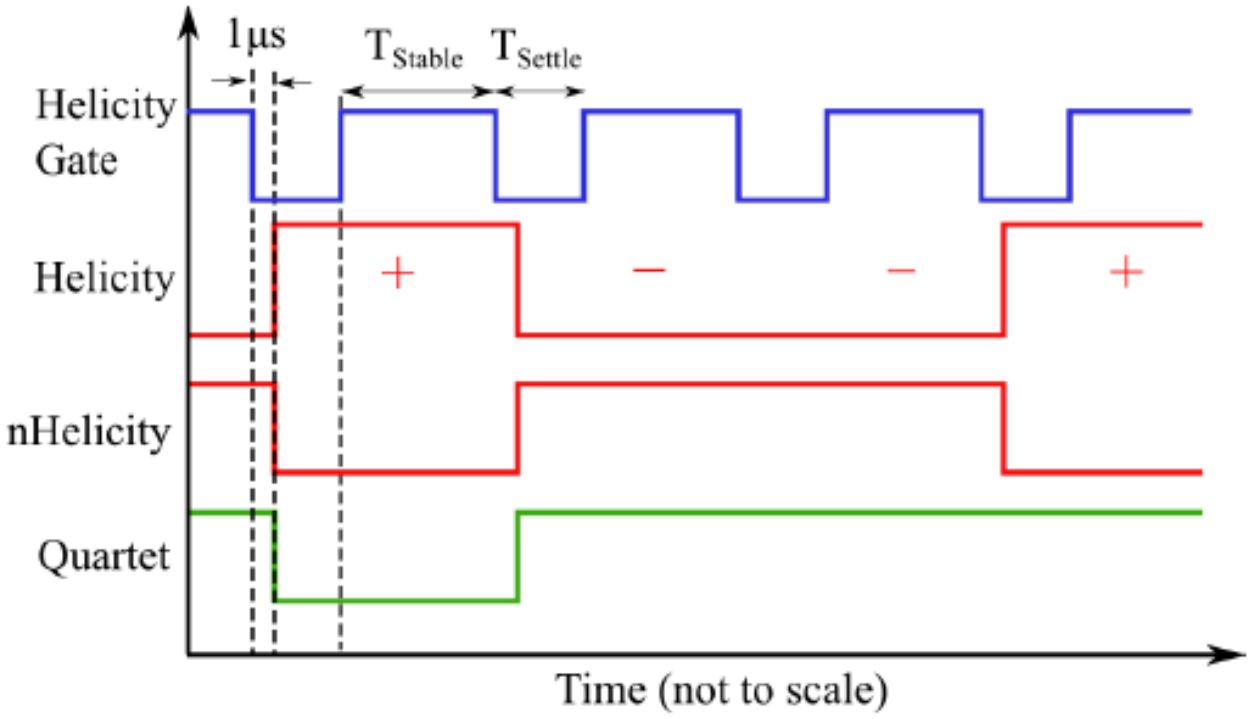
- Demonstrate integrating mode readout rate of 0.96 (1.92) kHz with pulser test.
- Stress-test data transfer to Mass-Storage System with > 500 Mbit/sec (> 1 Gbit/sec) pulser test.

These will be verified with the assembled DAQ system in stress tests.

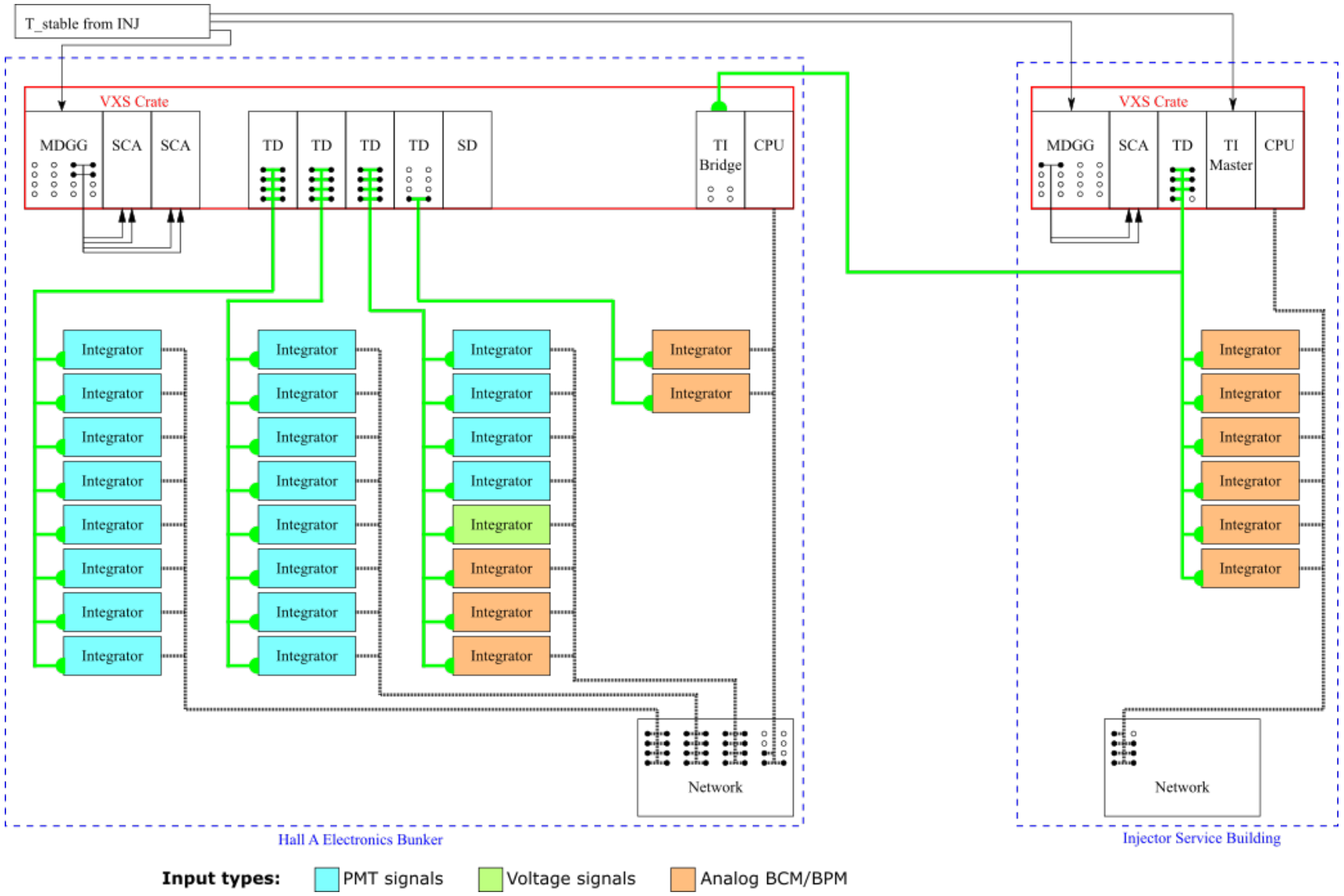
No Change since CD-1

Helicity windows and patterns

- Beam helicity is set in the injector and controlled by the helicity generator board
- Beam helicity is stable for ~500 μs with a 10-20 μs "T_{settle}" period, in which the helicity state changes
  - Data is not accumulated during T_{settle}
- Helicity windows are generated as a "pattern", in which the relative helicity states of the windows have a given pattern (e.g. quartets are +--+ or -++-)
  - MOLLER plans to use a 64-event pattern
- The starting helicity state of the pattern is generated using a 30-bit pseudo-random algorithm



Subsystem overview: integration DAQ



Helicity trigger is formed in ISB from Helicity Generator, so that INJ gate is formed promptly

Gate timing adjusted per TI node to account for ~20μs electron transit or other signal latencies; need ~0.1μs resolution

TI Bridge feeds SD/TDs to distribute gates/triggers

TI to Integrator connection use one QSFP connection

10Gb/s network on QSFP connections

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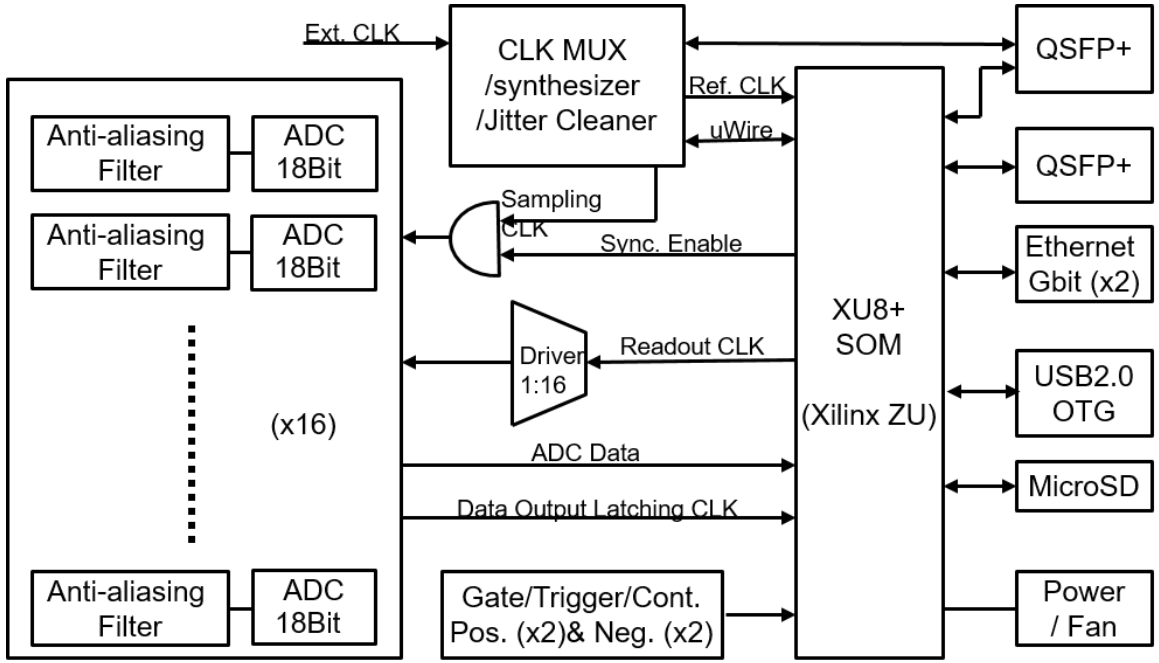
Integrating ADC design

16-channel sampling-integrating ADC

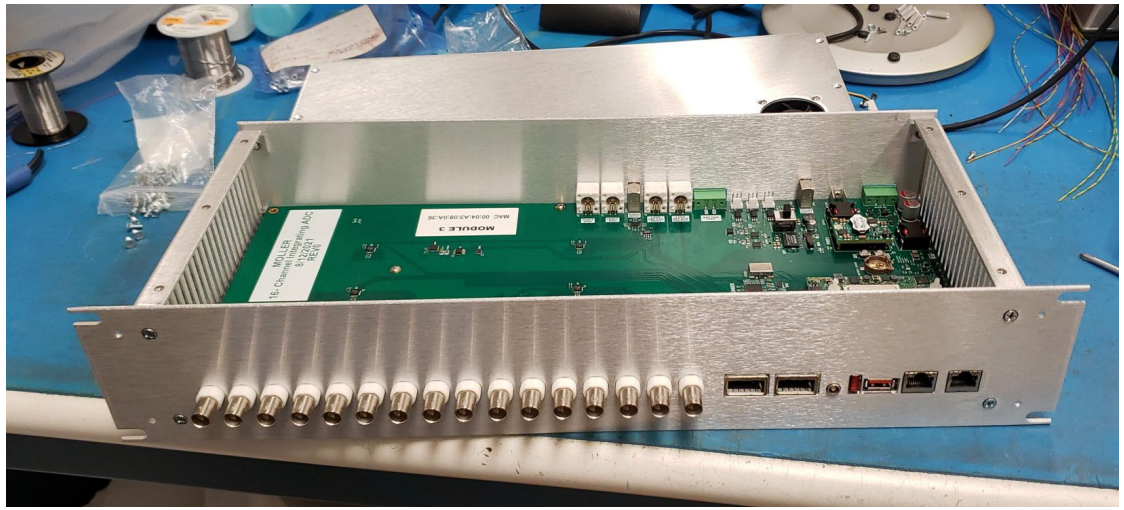
- Antialiasing filter limits bandwidth to 1 MHz
- 18-bit ADC clock runs at 14.7 MHz (250 MHz/17)
- FPGA sums the samples within the 500μs helicity window (~7352 samples)
- Production mode: sums over the helicity window and four equal-length sub-blocks
  - 32-bit values of sum, sum-of-squares, min, max, and number of samples reported for each block.
  - Data rate from 32 modules → 130MB/s
- Waveform mode: all samples are reported from selected channels
  - For Fourier analysis, need to be able to get all samples from about 1 continuous second



Jefferson Lab

Integrating ADC design

- Detector signals are differential on twin-ax connectors
  - Alternate input-stage allows for single-ended beam monitor signals on BNC connectors
- Clock and trigger signals come in from TI over optical QSFP connection
- Power supplied through Power over Ethernet (PoE) --- board needs 28W
- Optical QSFP will allow up to 10Gbps data transfer in streaming mode
- ADC board design reviewed by JLab staff
- Chassis has been designed and constructed at JLab

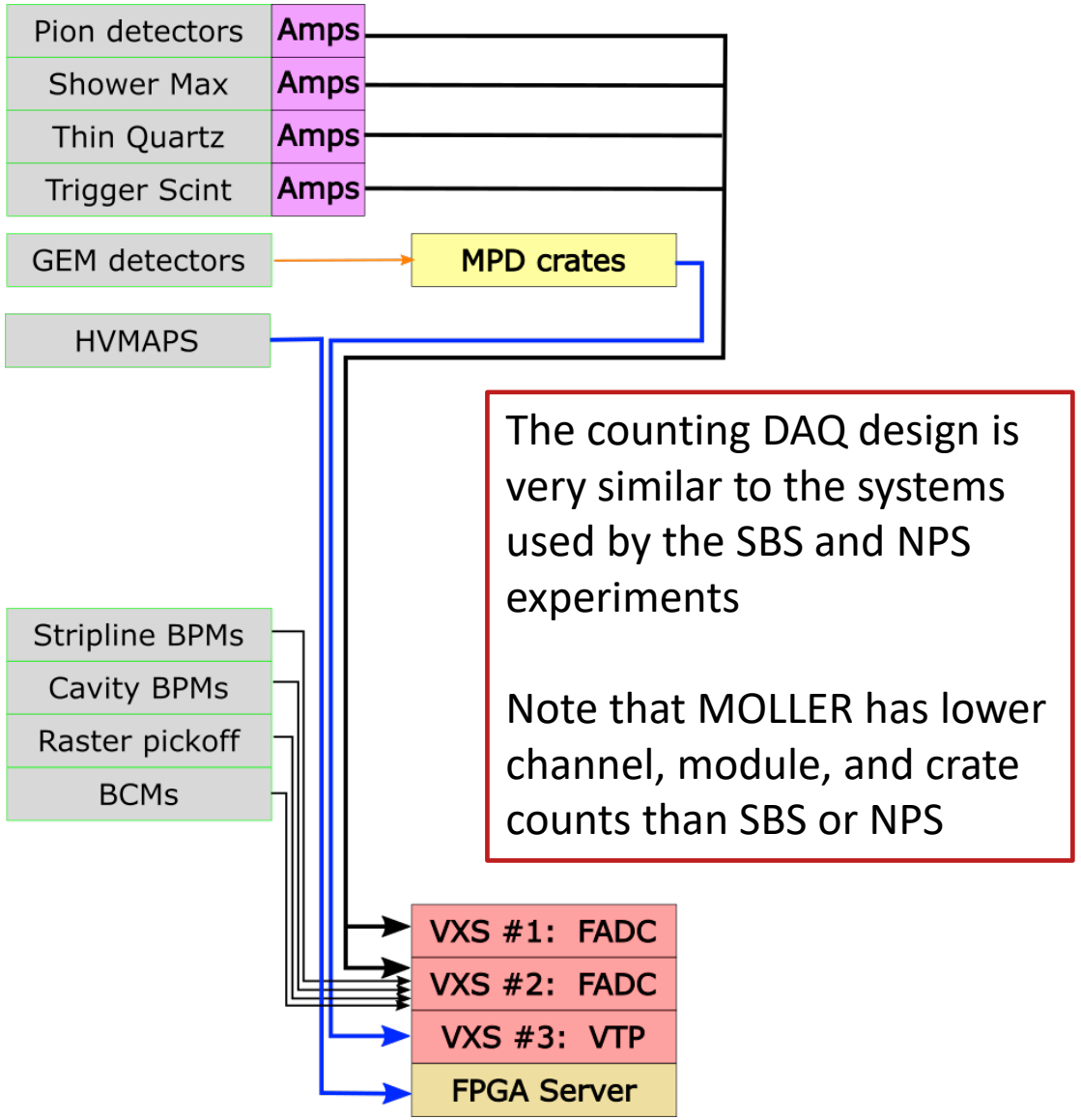


Data rate, file segment sizes, and data set size

- The standard data rate for the integrating DAQ will be about 130 MB/s
  - The data rate is independent of beam being on or off;
  - One hour of data would be about 470 GB
- A convenient size for the data file segments might be 20 GB → ~150 seconds
  - Hour-long runs would be split into about 23 segments

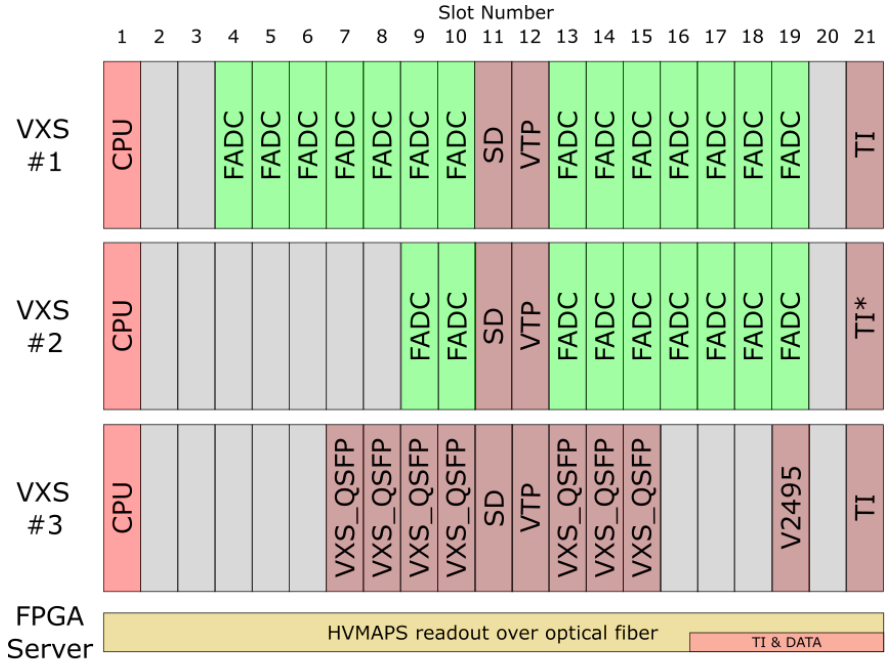
- The total data footprint for the entire experiment is 14PB
  - Production + Compton raw data: 9.5PB (main production DAQ, 8PB; Compton, 1.5PB)
  - Production + Compton analysis results: 2PB
  - Tracking raw data & analysis results: 1.5PB (raw data, 1.25PB; analysis results, 0.25 PB)
  - Simulation: 1PB

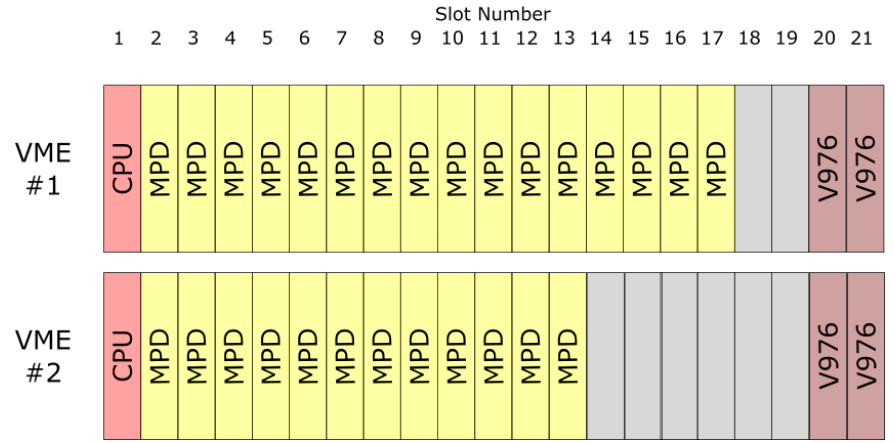
Subsystem overview: counting DAQ



The counting DAQ design is very similar to the systems used by the SBS and NPS experiments

Note that MOLLER has lower channel, module, and crate counts than SBS or NPS





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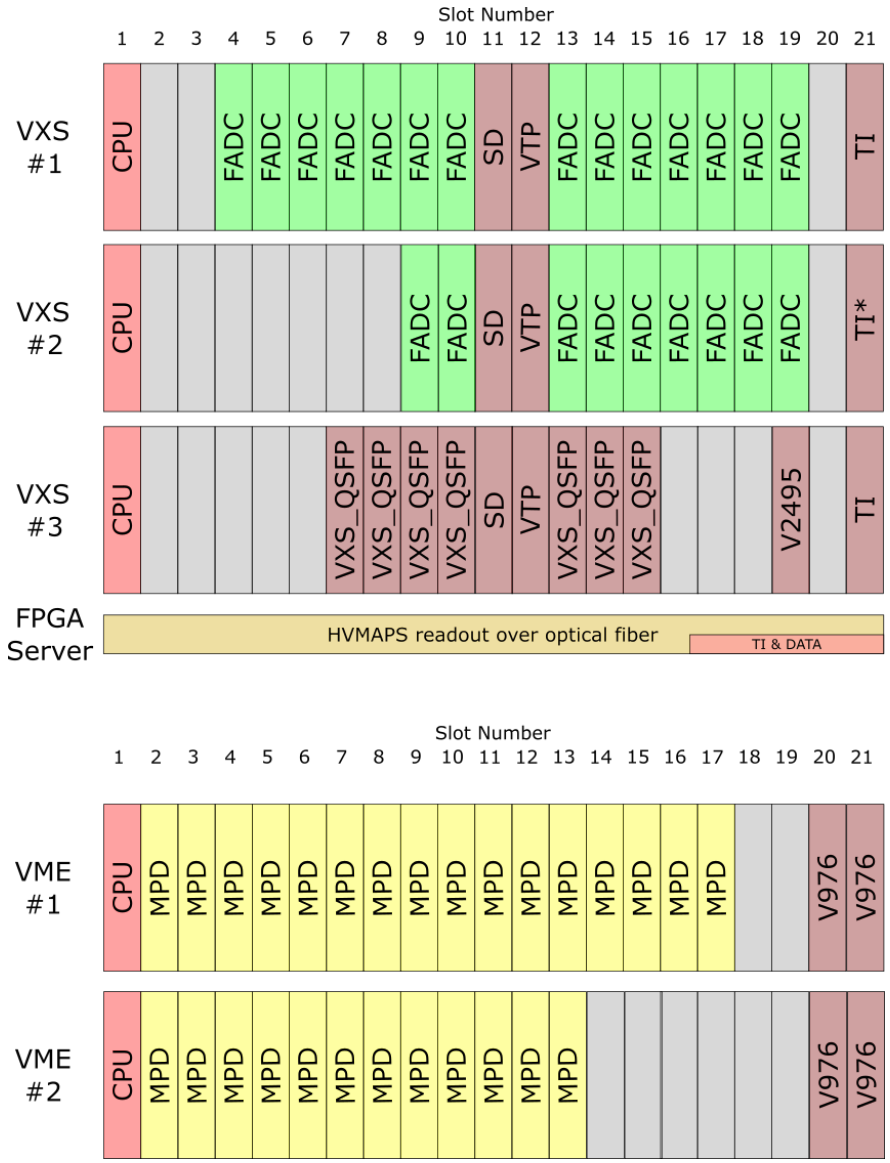
Counting mode trigger processing plans

- FADC modules stream hit data to VTPs
- VTPs in crates #1 & #2 select active trigger channels, transfer to VTP#1, form coincidences, and send event triggers to the TI-master
- TI-master accepts event triggers and sends triggers to the client TIs
- V2495 sends Clock and Trigger signals from TI to V976 fanout modules for the MPDs
- MPDs communicate over optical fiber to VTP in crate #3
- FADCs are readout over the backplane
  - Or may transfer through VTP QSFP



Jefferson Lab

Counting mode trigger plans

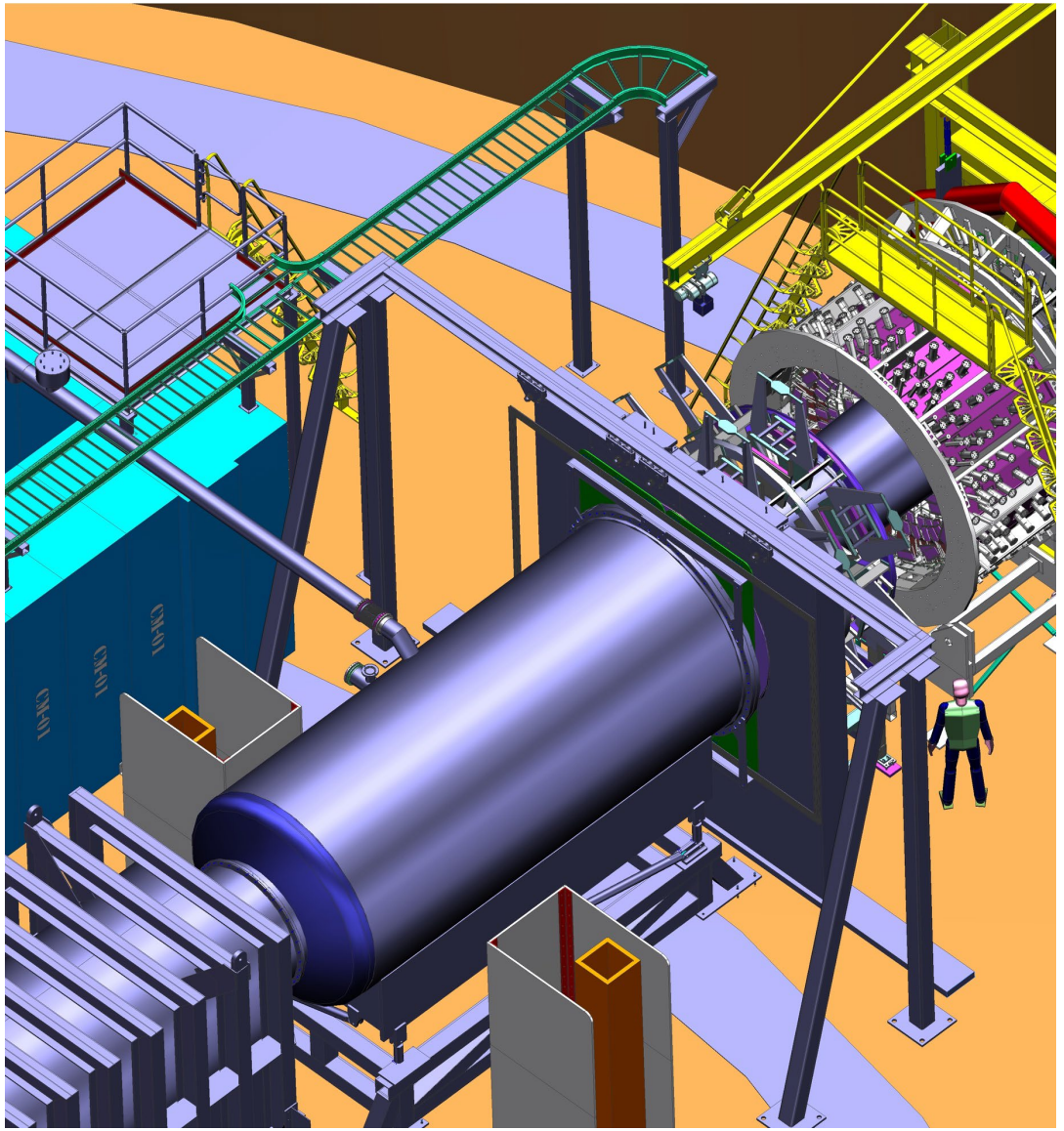
Desired modes for VTP-based trigger

1. Primary Counting-Mode Trigger
   - Trigger: "OR" of $i = 1,7$ of $[TS^{i}_{up} \cdot TS^{i}_{down}]$
2. Quartz-triggered mode
   - Triggers: possibility to select:
     a) OR of all thin quartz detectors in a given ring
     b) OR of all ShowerMax detectors
3. Pion-triggered modes
   - Triggers: possibility to select from:
     a) OR of all pion detectors
     b) [OR of all pion detectors] · [OR of all $TS^{i}_{up} \cdot TS^{i}_{down}$] (rate symmetry of pions; πTS efficiency; enhance pion signal)

- At "high" beam currents (~100 nA) can use a pulser trigger instead
  - Moller rate @ 100 nA is ~30MHz/sector, so there would be 3 hits/sector/100ns
- Coincidences between thin quartz detectors and scintillators can be selected in analysis, or can be used as a coincidence trigger
- Doing APV readout permits a maximum event rate of ~5 kHz.
  - If running without the GEMs we will be able to reach higher event rates

GEM Readout

- GEM modules will be instrumented by APV25 cards, which will be connected to MPD modules via HDMI cables
  - We have 10 APV per MPD (max is 15)
- Data from MPD modules will be transferred over optical cable to a VTP module
  - This is identical to the system currently in use by the SBS experiment
- MPD modules will be in shielded area near the detectors
  - Simulated total dose over the full experiment is a few krad
  - We are in communication with SBS to understand their radiation experience with the MPDs
  - To date, no APV or MPD failures have been attributed to radiation



Online Analysis

- Needed Tasks
  1. Helicity correlated (HC) feedback
     - Feedback cycle likely 10 s
  2. Monitor of data quality
     - Some issues only appear at high statistics, needing hours or days
     - Requires correction for HC beam properties
  3. Monitor of transverse beam polarization
     - Requires corrections for HC beam properties
     - Requires accumulating multiple hours of data
- Raw data files will be copied automatically to JLab Mass Storage System (MSS) tapes
- Computing hardware plans
  - One workstation for helicity-correlated feedback
  - Several workstations for full analysis to support #2 and #3
  - 200 TB fileserver provides space for 8-10 days of raw data and analysis results
    - Raw data rate is 450 GB/hr, full outputs are similar in size
- Will mostly use the existing workstations in CHA; MOLLER-NSF is procuring new analysis servers and 200 TB file server

Charge questions: DAQ

8. How is the DAQ and trigger system for the counting mode optimized to prevent bandwidth bottlenecks while ensuring the collection and transfer of 100% of the data without deadtime?

   What strategies are in place to minimize data acquisition delays, and what real-time monitoring tools are available to detect and correct inefficiencies?

   What diagnostic tools are available to analyze system performance and suggest improvements?

9. What is the data volume expected for this experiment?

   Would the experiment require large computing resources to process the collected data?

Charge questions: DAQ

8. How is the DAQ and trigger system for the counting mode optimized to prevent bandwidth bottlenecks while ensuring the collection and transfer of 100% of the data without deadtime?

The counting mode does not need to acquire 100% of the data and can tolerate deadtime and prescaling. Counting mode deadtime will also be adjusted using knobs such as the TI hold-off time and the size of the FADC sampling window

The integrating mode must be deadtime-free (except the spin flip) and must collect 100% of the data.

a) "Event triggers" are exactly periodic and based on the 500.85 μs+20 μs helicity gates

b) Each 16-channel ADC module contains its own readout controller, allowing internal data transfers to be faster than the Tsettle time, and keeping the data rate per 1 Gbps link at about 32.5 Mbps

c) The total data rate of 130 MB/s (~1040 Mbps) from the hall to the CHA servers will go over a pair of 10 Gbps links (trunk fiber will support change to 40 Gbps links)

Charge questions: DAQ

8. What strategies are in place to minimize data acquisition delays, and what real-time monitoring tools are available to detect and correct inefficiencies?

   What diagnostic tools are available to analyze system performance and suggest improvements?

Integration mode:

There will be active monitoring for missed helicity events in both front-end hardware scalers and in the data analysis.

This has been done on all recent parity experiments (Qweak, PREX-II, CREX)

Both Integrating and Counting mode:

Standard live-time and data rate monitoring tools within the CODA system will be used, similar to previous experiments including SBS

Charge questions: DAQ

9. What is the data volume expected for this experiment?

   Would the experiment require large computing resources to process the collected data?

Over the full course of the experiment (101 weeks as in PAC37 update), the total data volume is about 14 PB.

- Raw data volume during production running: 9.5 PB (1.5 PB from the Compton)
- Integration mode and Compton polarimeter analysis results: 2 PB
- Counting mode raw data and analysis results: 1.5 PB.
- Stored data from simulations: 1 PB

The offline analysis on the farm machines is projected to be at or slightly above the Hall A “fair share”

Paul King

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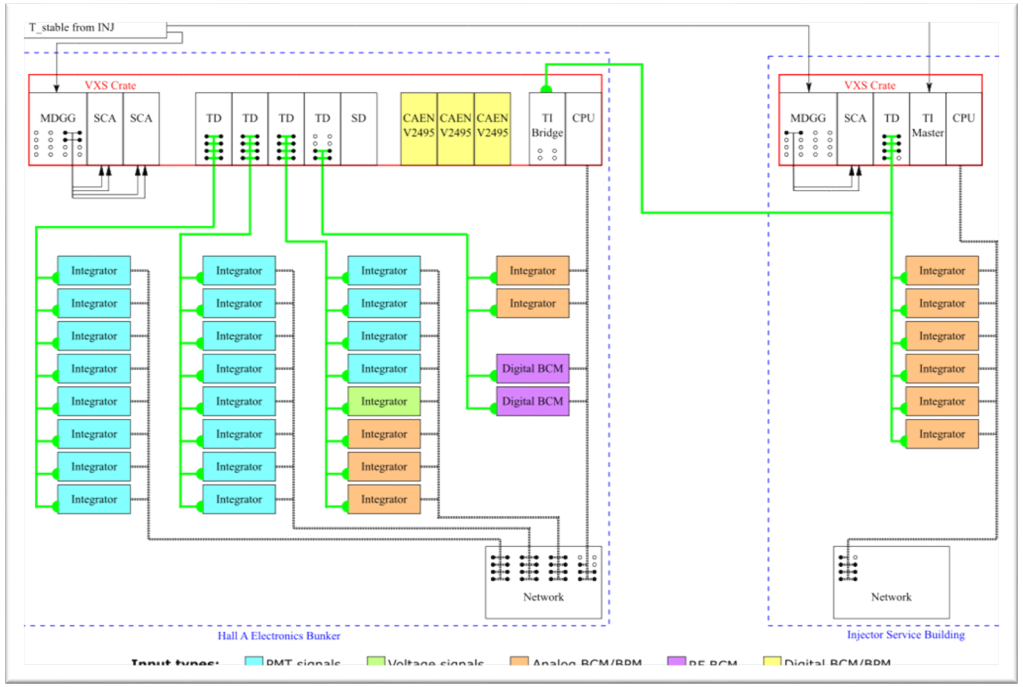
Summary

- Nearly all DAQ hardware is at JLab (some is still at OhioU)
  - Computing procurements and interconnection cables are in process
- Firmware development for the integrating ADCs had been slowed in part due to the tariff-related delays in shipping the rev2 boards to JLab
  - All rev2 ADCs are expected at JLab imminently
- Multiple test stands of both systems in use, allowing build up for the assembly in early fall



Appendix slides follow

Requirements of the DAQ and Trigger for MOLLER

- Integrating mode DAQ & Trigger -- Production Mode
  - Detector & Monitor signals integrated (summed) during each helicity window.
  - Collect and transfer 100% of the helicity window data, without deadtime.
  - Conceptually similar to previous Parity experiments.
- Counting Mode DAQ & trigger -- for checking Kinematics, Backgrounds, Alignment.
  - Detector & Monitor signals read in event mode at 10 to 300 kHz
  - Triggers based on scintillators or detectors or a pulser.
  - Similar to the SBS DAQ
- Event building & online analysis
  - Integration mode data rate of 130 MB/s
  - Helicity-correlated feedback must occur with ~100% throughput.
  - Fully-correlated asymmetry analysis with ~100% throughput.
  - Disk storage to hold results spanning several days

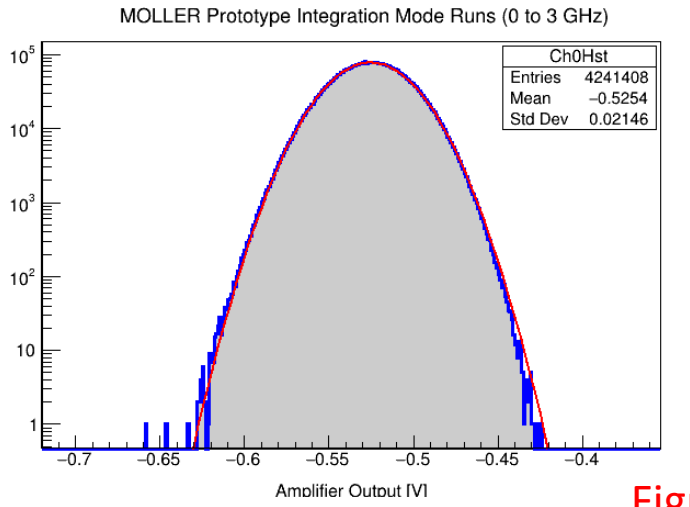
Integration ADC development history

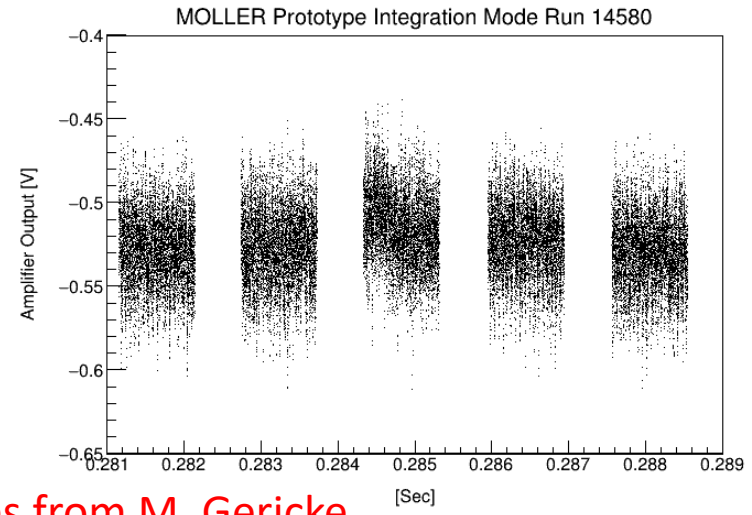
U. of Manitoba and JLab scientists have actively collaborated with TRIUMF and JLab engineers throughout the development. JLab engineers developed the CODA interface for the boards.

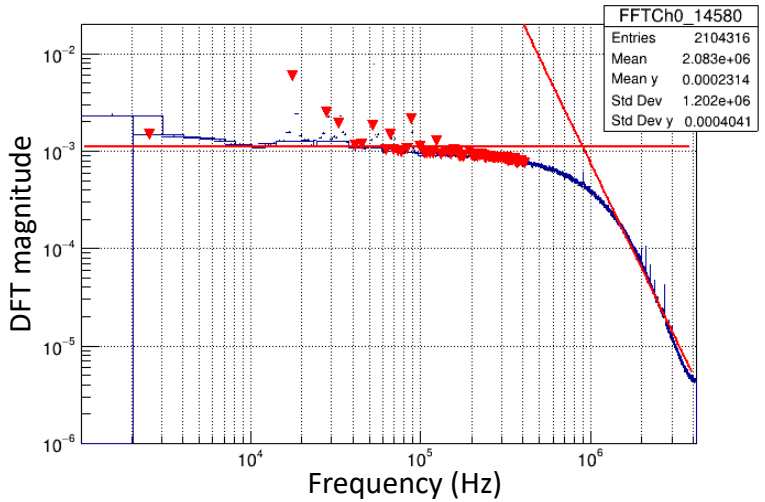
- Revision 0
  - First 16-channel version of the integrating ADC
  - Used in Mainz beam tests in 2021-2022
  - One at JLab allowing CODA integration to begin
- Revision 1: 10 boards produced Fall 2023
  - Actively used in testing at Manitoba, Idaho, JLab, TRIUMF
  - Major development work on firmware and CODA support
- Revision 2: 10 boards produced late Fall 2024
  - First 25% of the production order
  - A board assembly (BOM) issue was found at end of December
  - Resolved by exchange of one component
- Production run of rev2 was completed during the spring (total of 40 modules); delivery of the modules to JLab was delayed due to tariff issues
  - 3 modules arrived in early June
  - Additional 31 modules due to arrive shortly
  - Remaining modules are going through final testing at Manitoba

Results from the integrator ADC (rev0) during 2021 Mainz tests

- The integrating signal level is gaussian except for beam excursions
- Initial firmware gave 8191 samples over $\simeq 0.983\ ms$ with about $\simeq 0.5\ ms$ break between sample – next version allowed full sampling rate at $\simeq 15\ Msps$
- The high sampling rate allows us to run DFTs in diagnostic mode and identify potentially troubling noise sources and beam problems.







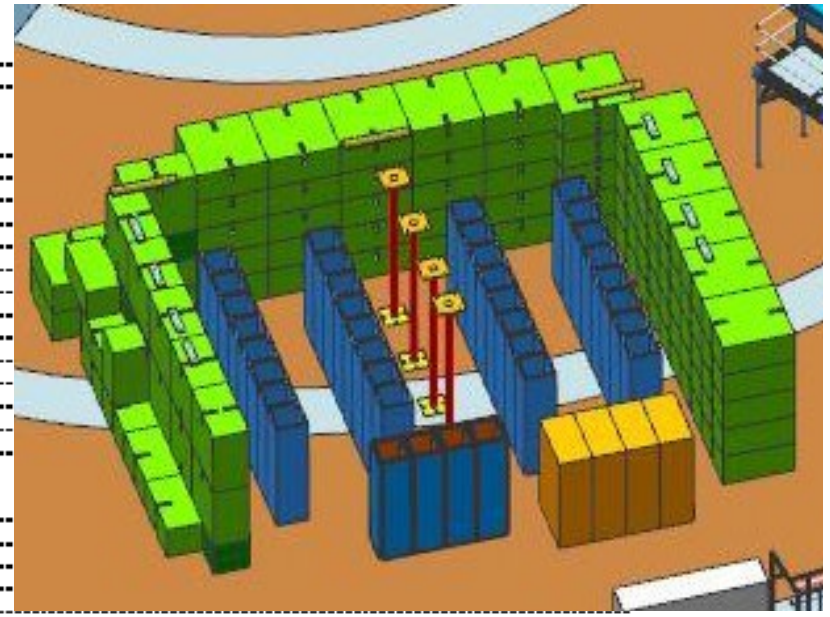
Figures from M. Gericke

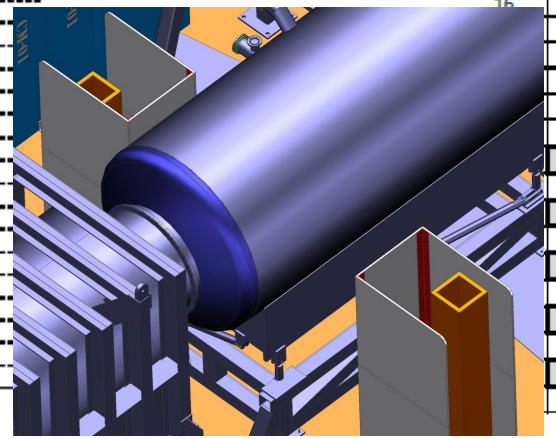
Jefferson Lab

Planned DAQ rack layouts

U position	Row1, Rack 1	Row1, Rack 2	Row1, Rack 3	Row1, Rack 4	Row1, Rack 5
42	Fiber optic trunk patch for TI Bridge	PoE++ Switch, 48 ports, 1980 W output		Fiber optic trunk patch for MPDs	RG58 to Lemo patch panel
41					
40		SFP Network switch, 32 x QSFP28	Console server		
39				Counting mode VTP crate	
38	MOLLER ADC 10		MOLLER ADC 26		
37					
36		MOLLER ADC 16			
35					
34	MOLLER ADC 09		MOLLER ADC 25		
33					
32		MOLLER ADC 15			Counting mode VXS FADC crate #1: 14 FADC -- thin quartz
31					
30	MOLLER ADC 08		MOLLER ADC 24		
29					
28		MOLLER ADC 14			
27					
26	MOLLER ADC 07		MOLLER ADC 23	Fiber optic trunk patch for HVMAPS	
25					
24		MOLLER ADC 13		Arista switch (HVMAPS)	
23					
22	MOLLER ADC 06		MOLLER ADC 22		
21					
20		MOLLER ADC 12			
19					
18	MOLLER ADC 05		MOLLER ADC 21		RG58 to Lemo patch panel
17					
16		MOLLER ADC 11			
15					
14	MOLLER ADC 04		MOLLER ADC 20		
13					
12					
11					
10	MOLLER ADC 03		MOLLER ADC 19		
9					
8					
7					
6	MOLLER ADC 02	Integration mode VXS trigger crate	MOLLER ADC 18		Counting mode VXS FADC crate #2: ~10 FADC --- ShowerMax, Pion, Beamline, etc
5					
4					
3					
2					
1	MOLLER ADC 01		MOLLER ADC 17		

Row2, Rack 6	Row2, Rack 7	Row2, Rack 8	Row2, Rack 9	Row2, Rack 10
MPD crate location during initial DAQ checkout	MPD crate location during initial DAQ checkout			





U position	Beam Left	Beam Right
42	MPD VME Crate 1	MPD VME Crate 2
41		
40		
39		
38		
37		
36		
35		
34		
33		
32		
31	Fiber optic trunk patch for MPDs	Fiber optic trunk patch for MPDs
30		
29		
28		
27		
26	GEM LV supply	GEM LV supply
25		
24		
23		
22		
21		
20		
19		
18		
17		
16		
	PSU 150-10 #1	PSU 150-10 #2
	PSU 6-200 #7	PSU 6-200 #8
	PSU 6-200 #5	6PSU 6-200 #6
	PSU 6-200 #3	6PSU 6-200 #4
	PSU 6-200 #1	PSU 6-200 #2

Procurement status

Procurement for DAQ and Trigger is largely in the NSF and CFI scope, and is nearly complete

- VME & VXS crates---2 VME & 6 VXS crates and 8 VME CPUs are in hand
- Integrating ADCs--- 34 rev2 modules have been tested and are at or en route to JLab
  - —3 of them are on-site already
- Fiber cable for ISB→Hall TI connection
  - —Both the ISB→CHA fiber cable and the CHA→HallA fiber cable have been installed
- Network switches, for both fiber SFP and PoE are in hand
  - —SFP transceivers being tested with the integrating ADCs & our switch
- TI/TD/SD---six TI, six TD and 6 SD are in-hand
- VTP modules---All 3 are in-hand, VXS_QSFP expansion cards at JLab
- Support modules: Scalers & V2495 are in-hand
- FADC modules---All 28 modules are at JLab, and are in use in the ESB test stand
- MPD modules from SBS will be used
- Computing procurements planned to occur very shortly

ES&H and Quality Assurance

- Electrical safety
  - Wherever possible UL listed electrical components will be used
  - Integrating ADCs and other custom electronics (non-NRTL) will be reviewed by the JLab Electrical Safety Subject Matter Expert and registered
- Quality Assurance
  - We will test every board and module
  - Combined system tests will be done on individual subsystems and the full system
  - Full system tests will be used to verify the KPPs and deliverables

Analysis software

Analysis software is not in the project scope, but impacts decisions such as the computing hardware needed for the online analysis.
Major development started last year, but building on prior experiments

Integrating analysis framework

- Building on the “japan” (Just Another Parity Analyzer) framework used by PREX/CREX and Qweak
- Mock-data generator within japan allows benchmarking of analyzer performance with a model data-stream similar to that expected from the full DAQ
- Currently adding further complexity to the mock-data to develop the tools which will be needed by shift crews and experts

Counting analysis framework

- Starting with a version of the Hall A “Podd”-based analysis package used by SBS
- The FADC decoding classes are in use in the counting test-stands in the Test Lab and at William and Mary
- The GEM decoding classes have been tested with data from the GEM test stand
- Continuing to adapt detector array and track-finding classes for the MOLLER detectors and geometry

Online feedback

- An independent realtime process
  - Connects to the live data stream
  - Calculates charge asymmetries and position differences; averages these over short time scales
  - Determines modified values for INJ control devices (RTP cell, helicity magnets, …) to correct the HC beam parameters to zero and communicates these via EPICS
  - Status:
    - Existing feedback algorithm as used in PREX/CREX and Qweak is still operational
    - Algorithm supports different time-scales for charge and position feedback

Backup slides follow

How is MOLLER Counting different than “usual” Hall A/C experiments

- In Counting mode, nearly 100% of the triggered events are expected to be "good" Moller or e-p events, each of which could be a valid event written to tape.
  - Even scaling down the beam current from 65 muA to an ultra-low value of 200 pA the total rate of these good events would be 100 KHz, too many to record without deadtime. So, we will be prescaling the triggers significantly.
- For a typical counting mode configuration (target, rotational angle of the rotator, beam energy) we would only require a few million events to tape. Assuming the DAQ max throughput is 4 kHz we would get those statistics in a few minutes of beam.
- The overhead to change configurations would likely by much more than the data-taking.
- So, we will pre-scale the counting DAQ triggers significantly, and the only issue is that we want to be able to know the deadtime after the prescaling so that we can normalize between different runs.

Comparing the MOLLER counting DAQ and SBS

MOLLER counting DAQ

- Two FADC crates with VTP triggering
  - Baseline plan is VME readout, but readout through VTP is possible
- One VTP crate for GEM readout
  - 7 VXS_QSFP cards (28 MPD cards)

SBS GEp-V

- Nine FADC crates with VTP triggering
  - ECAL: 7 crates using VME readout
  - HCAL: 2 crates readout through VTP
- Four VTP crates for GEM readout
  - 8-12 VXS_QSFP cards per VTP (32-48 MPD cards for each VTP)
- Three VME crates without VTP for CDet and beamline
- One TS crate

Thought on optimizing the deadtime in counting mode

- The MOLLER counting DAQ will be used to commission MOLLER detectors at the beginning of the run and occasionally to study background. There is no need to transfer 100% of the trigger-associated data; we can prescale, if needed, to bring the dead time to an acceptable level.
- Also, there are "knobs" we can turn to minimize dead time such as the TI hold off time and the size of the FADC sampling window.
- In addition, we are considering transferring the FADC data through the VTPs QSFP ports instead of the CPUs, if needed, as this mode of transfer is faster.

- There will be dead time studies on the bench where we will simulate the MOLLER expected detector rates (up to 300 kHz) with pulsers and the parameters mentioned above will be fine tuned that way before beam running as to minimize the time spent on dead time optimization once beam comes.

MOLLER Counting DAQ Dead Time Studies: Plan

The MOLLER counting DAQ setup: 2 VXS crates with VTP-based triggering

- VXS crate 1: all quartz main detector channels (**228**) in 15 FADCs
- VXS crate 2: Scintillator (28), Shower max (28), Pion Detector (28), Upstream Scanner (2) – **86** channels total in 6 FADCs
- VTP-2 will transfer to VTP-1 all FADC samples over threshold for all channels in VXS 2. All trigger logic will be done on VTP-1 with all detector channels available.

Dead time studies on the bench:

→ Copies of pulses generated by a random pulser will populate FADC channels to simulate the passage of a particle through a MOLLER global sector: 4 scintillator channels, 4 quartz channels, 1 shower max channel, 1 pion detector channel and 2 Upstream Scanner channels – **12** channels total (we can do more, if needed)

→ The live time monitored will be that calculated by the TI from incoming and accepted triggers

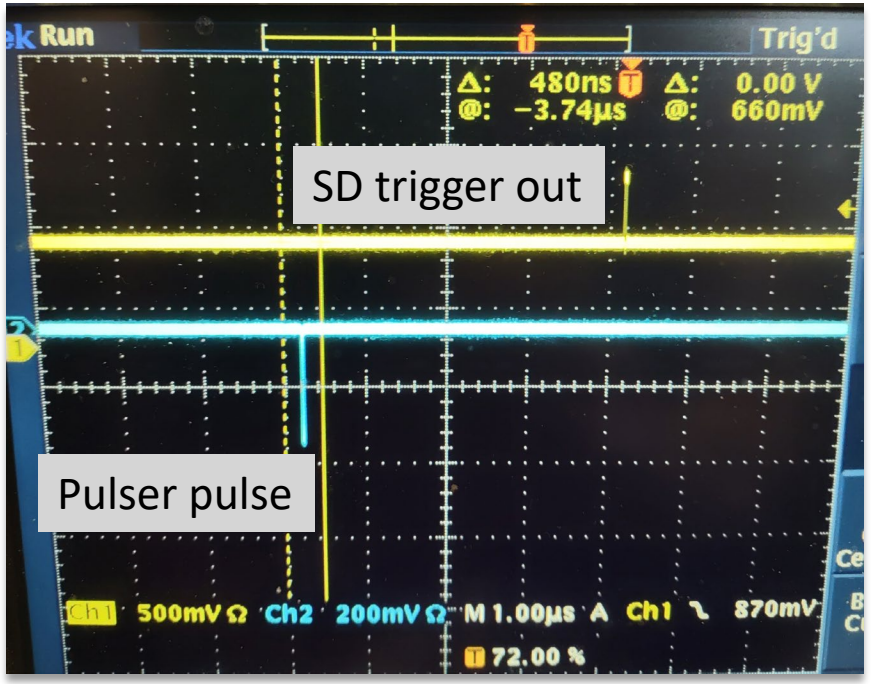
→ The TI live time will be monitored for various configurations where the following parameters will be varied: pulser rate, TI hold off time, FADC sampling windows, transfer of FADC samples once a trigger is accepted either through the CPU or through the VTP's QSFP port, zero suppression enabled or disabled. All this will be ultimately done with the full v3 FADC load for the 2 VXS crates.

These exhaustive studies will map the live time behavior of the MOLLER counting DAQ system ahead of beam arrival and it will allow for an informed selection of initial operating parameters.

Status:

→ 2 VXS crates have been set up in the ESB to initiate dead time studies

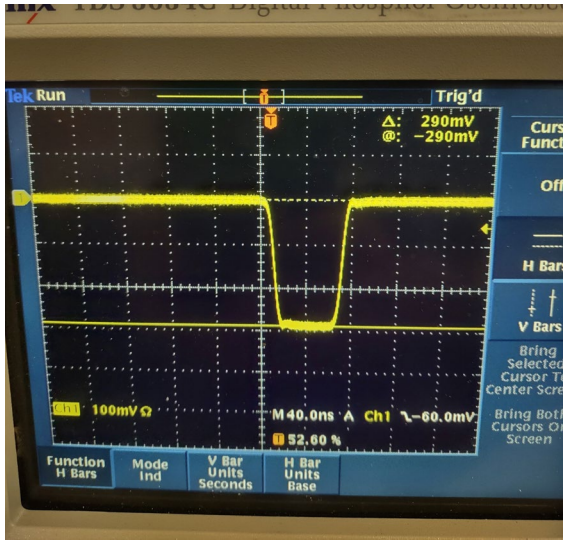
→ The firmware that allows the FADC v3 boards to communicate with VTPs is not released yet. For now “proof of principle” studies will be carried out with v2 boards and not at full load. The v3 boards firmware will be available very soon and by the time the 2 MOLLER counting DAQ VXS crates will be installed in Hall A (beginning to mid September) the dead time tests can proceed as outlined in previous slide.

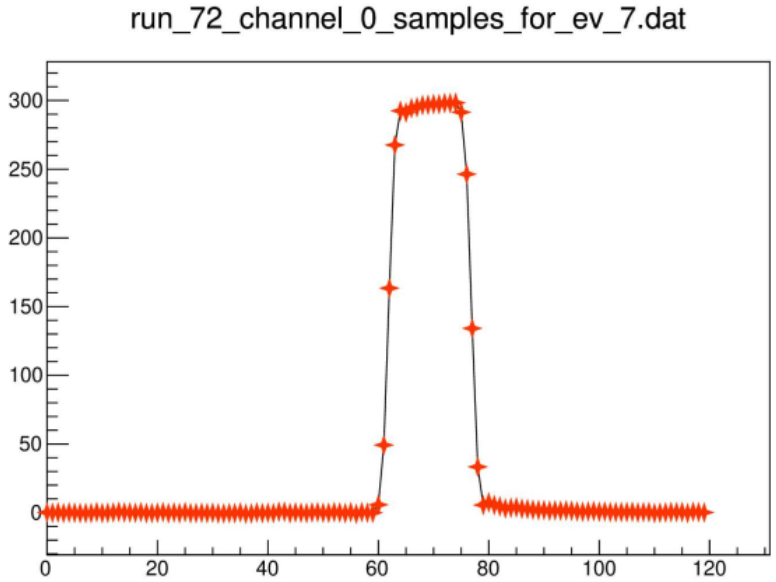


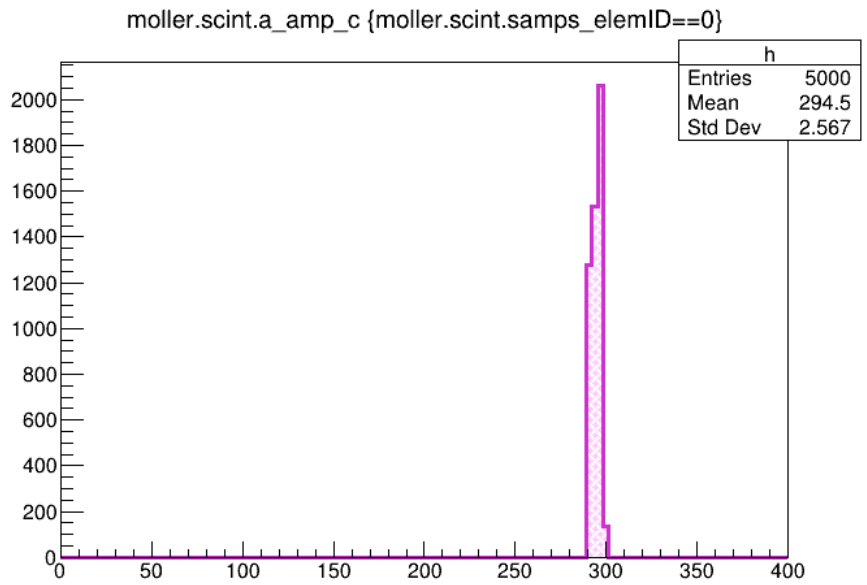
Counting DAQ testing in the ESB

Testing of the multi-VTP-crate triggering

- Fan-out of a pulse into four FADCv2 channels, two in one crate and two in the other
- VTP in each crate forms a 2-fold coincidence and sends a trigger to the TI input
  - Triggers from both crates are active
  - Each channel has FADC waveform and amplitude matching the input signal
- Next step: Connect the two VTP modules to form a 4-fold coincidence in the main VTP







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CEBAF Online Data Acquisition (CODA) Overview

CODA is a data acquisition framework developed at JLab which uses standard JLab-built hardware and software components

- Trigger Supervisor (**TS**) or Master Trigger Interface (**TI-Master**): Acts as the central control point for data acquisition; processes trigger inputs and frontend busy signals, then distributes clock, trigger and sync signals to the frontend electronics.
- Trigger Distribution (**TD**) & Signal Distribution (**SD**) boards: Fan out the clock, trigger, and sync signals from the TS to the TI boards and frontend modules (such as ADCs and TDCs)
- Trigger Interface (**TI**): Communicates with the TS (through a TD) to allow frontend modules to process a trigger, and the ROC to synchronize data event generation
- Read Out Controller (**ROC**): Software subsystem running on a frontend CPU (such as VME) which is responsible for readout of the frontend electronics and packaging the data as an event fragment for network transport; each ROC has an associated TI
- Event Builder (**EB**): Software subsystem running on a central server which assembles the fragments of each event via network transport from the ROCs and produces the combined datastream

Acronym dictionary

- **PoE**: Power over Ethernet; supplies low-voltage, low-current power over an Ethernet cable
- **MPD**: Multi Purpose Digitizer; a multiplexed ADC module, used with the APV25 (analogue pipeline ASIC) cards to readout the GEM modules
- **HVMAPS**: High Voltage Monolithic Active Pixel Sensors; a pixel detector in which the readout electronics are embedded within the pixels
- **VETROC**: VXS-based Electron Trigger and Readout Card; this acts as a TDC and can contribute to FPGA-based trigger formation in the VTP
- **VTP**: VXS Trigger Processor; FPGA-based module which uses data from other VXS/VME modules to form an event trigger; can alternately be used as a data concentrator with the MPD modules
- **NPS:** Neutral Particle Spectrometer; the collaboration and experimental program installed in HallC in 2023-2024
- **SBS**: Super Bigbite Spectrometer; the collaboration and experimental program currently installed in Hall A
- **BCM**: Beam Current Monitor; a beam-line element used to measure the electron beam current

Outline

- Physics needs and requirements
- Helicity windows and integration
- Overview of integrating DAQ
- Integrating ADC design
- Overview of counting DAQ
- Counting DAQ trigger
- GEM and HVMAPS readout
- Online/prompt computing
- ES&H and Quality Assurance
- Procurement status
- Summary

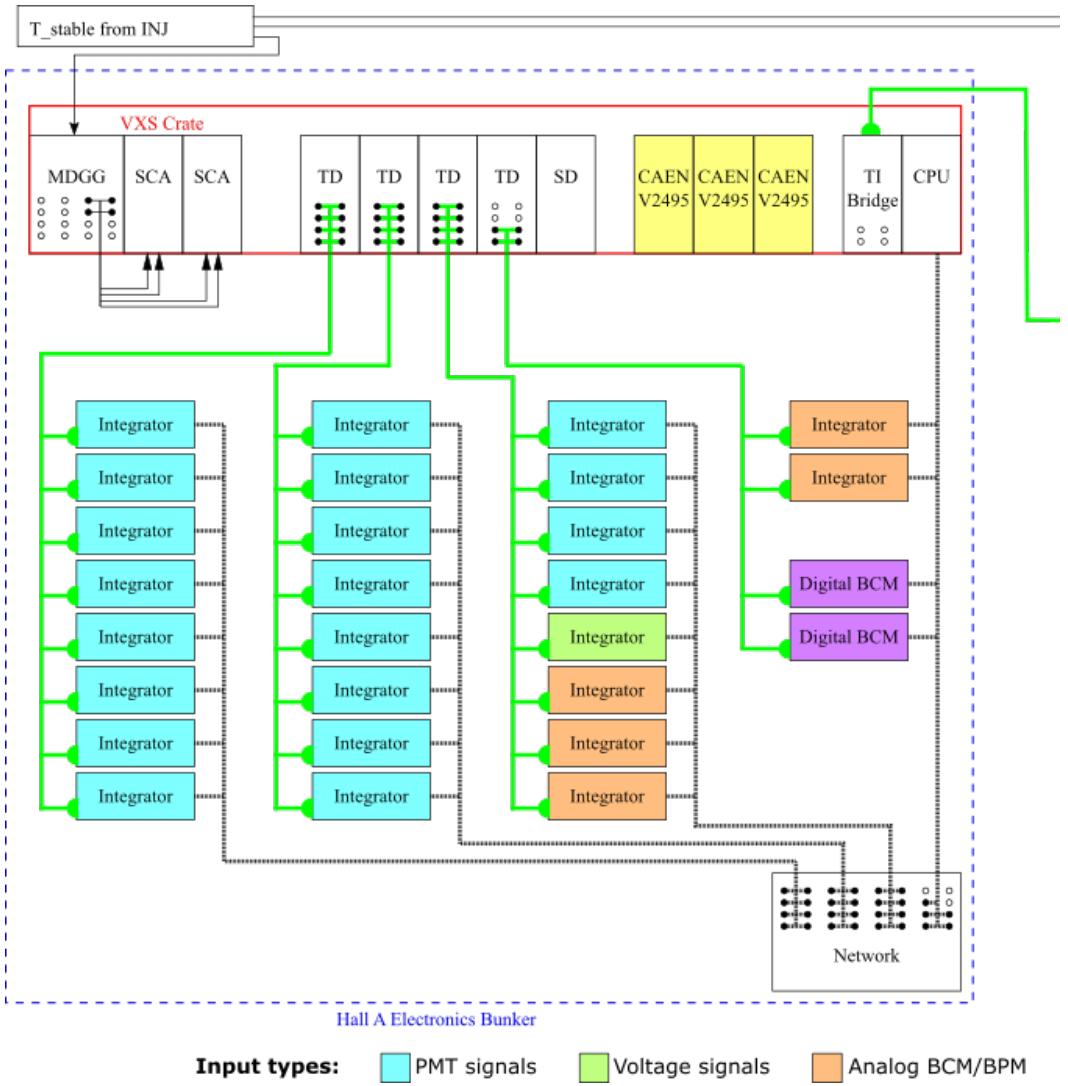
- Team Members:
  - L2 Manager, Control Account Manager
    - Robert Michaels, Jefferson Lab (retiring)
    - Simona Malace, Jefferson Lab (new CAM)
  - L2 Technical Lead
    - Paul King, Ohio University
  - Technical contributors
    - Michael Gericke, U. Manitoba
    - Jie Pan, U. Manitoba
    - David Armstrong, William and Mary
    - Sayak Chatterjee, U. Massachusetts
    - Chandan Ghosh, Jefferson Lab
    - Bryan Moffit, Jefferson Lab
    - William Gu, Jefferson Lab
    - Daryl Bishop, TRIUMF
    - Bryerton Shaw, TRIUMF
    - Arindam Sen, Ohio University

DAQ development contributors (based on DAQ meeting participation)

- D. Adhikari
- D. Armstrong
- J. Arrington
- D. Bishop
- B. Blaikie
- S. Chatterjee
- R. Conaway
- C. Cuevas
- J. Datta
- I. DeBord
- K. Dehmelt
- J. Dutta
- R. Fair
- M. Gericke
- C. Ghosh
- W. Gu
- Z. Ji
- P. King (TL)
- Y. Kolomensky
- S. Kundu
- Z. Li
- H. Liu
- S. Malace (CAM)
- D. McNulty
- Y. Mei
- R. Michaels
- B. Moffit
- B. Moran
- J. Mott
- J. Pan
- C. Pearsen
- B. Raydo
- S. Regmi
- A. Sen
- B. Shaw
- J. Shirk
- E. Sichtermann
- P. Souder
- S. Tarafdar
- B. Waidyawansa
- C. Zorn

Some details of the Integration DAQ

- Each 16-ch. integrator is an independent readout controller
  - Trigger fanout and synchronization are through the TI connections, allowing adjustment for latency differences
    - Beam transit from INJ to Hall ~21 μs
    - BCM/BPM latency w.r.t the detector
  - Sample clock will run at (250 MHz/17) ~14.71 MHz
- Data structure: in each helicity window and four equal-length “subblocks”
  - Sum
  - Sum of squares
  - Minimum and maximum sample value
  - Number of samples
- Streaming mode: can get all samples from a few channels



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Signal levels at the ADC input

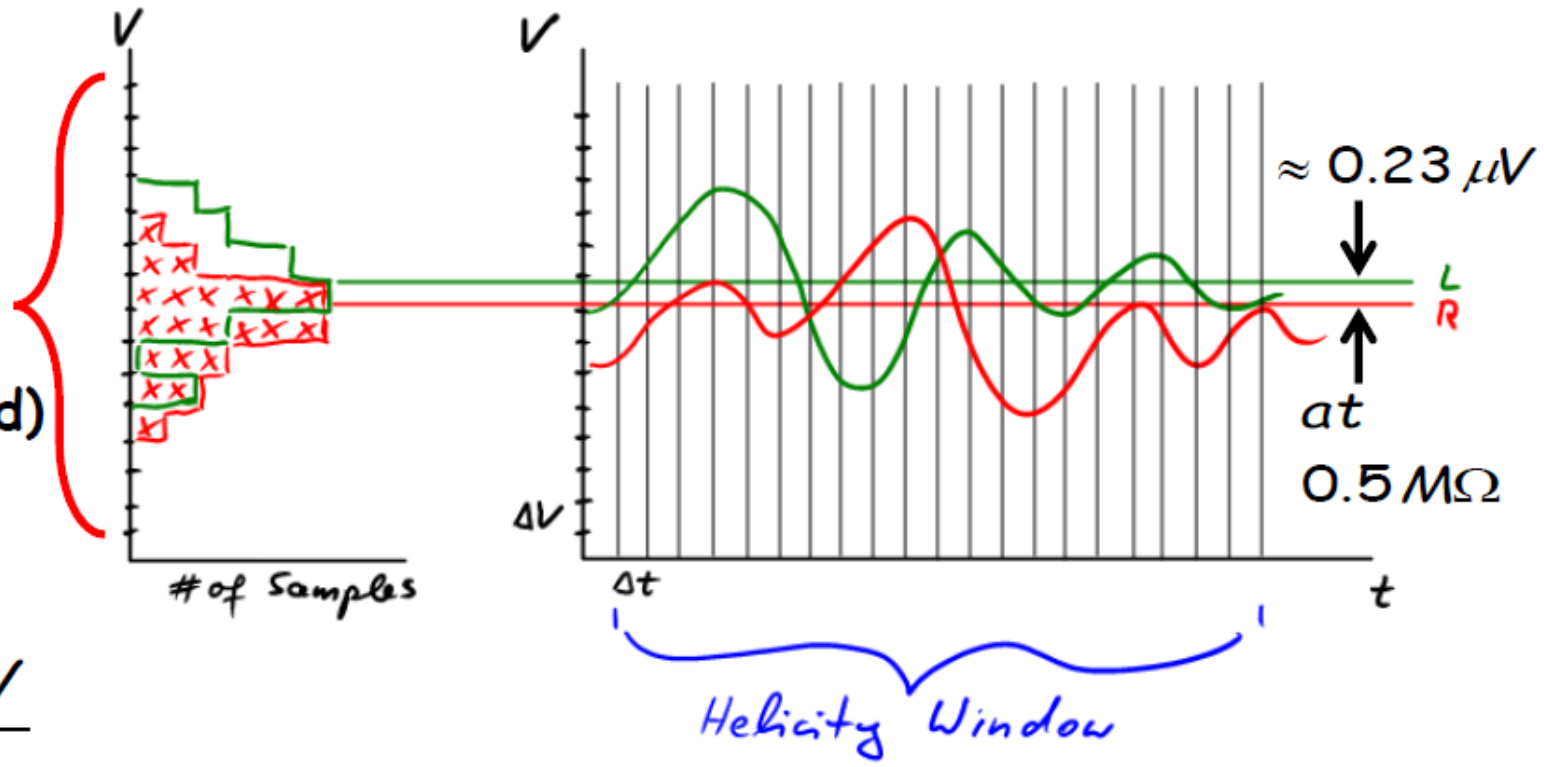
Digitization:

ADC range and resolution (0 suppressed)

18 bit Resolution:

$$\Delta V = \frac{10\,V}{2^{17}}$$

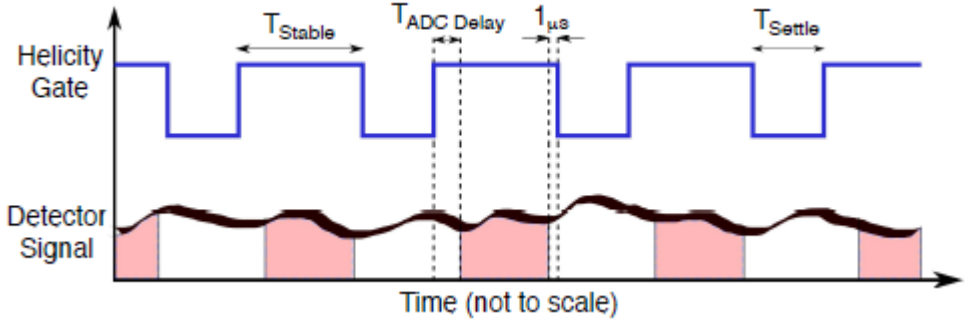
$$\approx 76\,\mu V$$

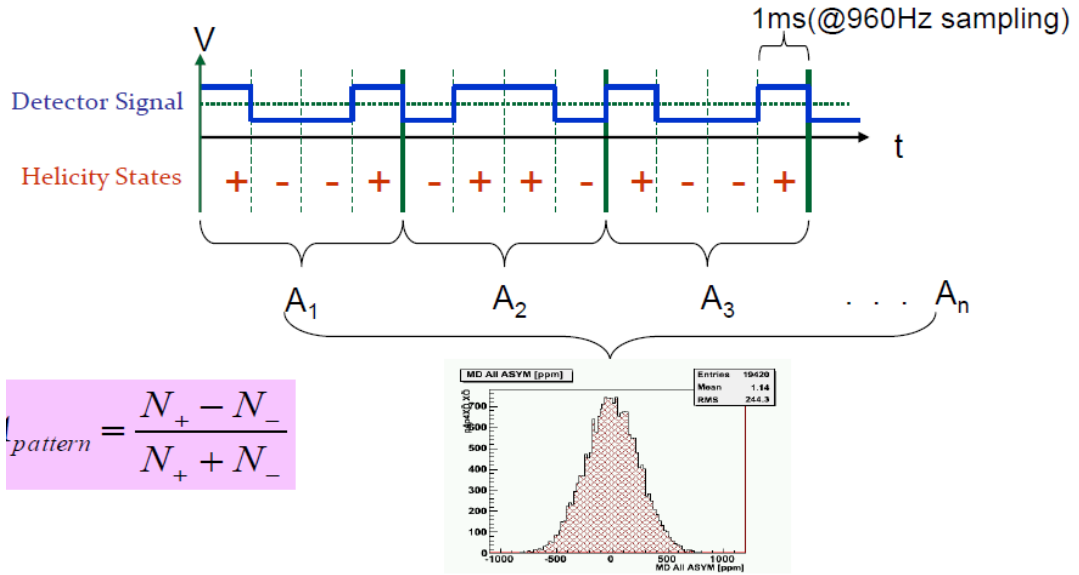


Signal RMS is spread over ~1200 ADC channels

Helicity windows and ADC integration scheme

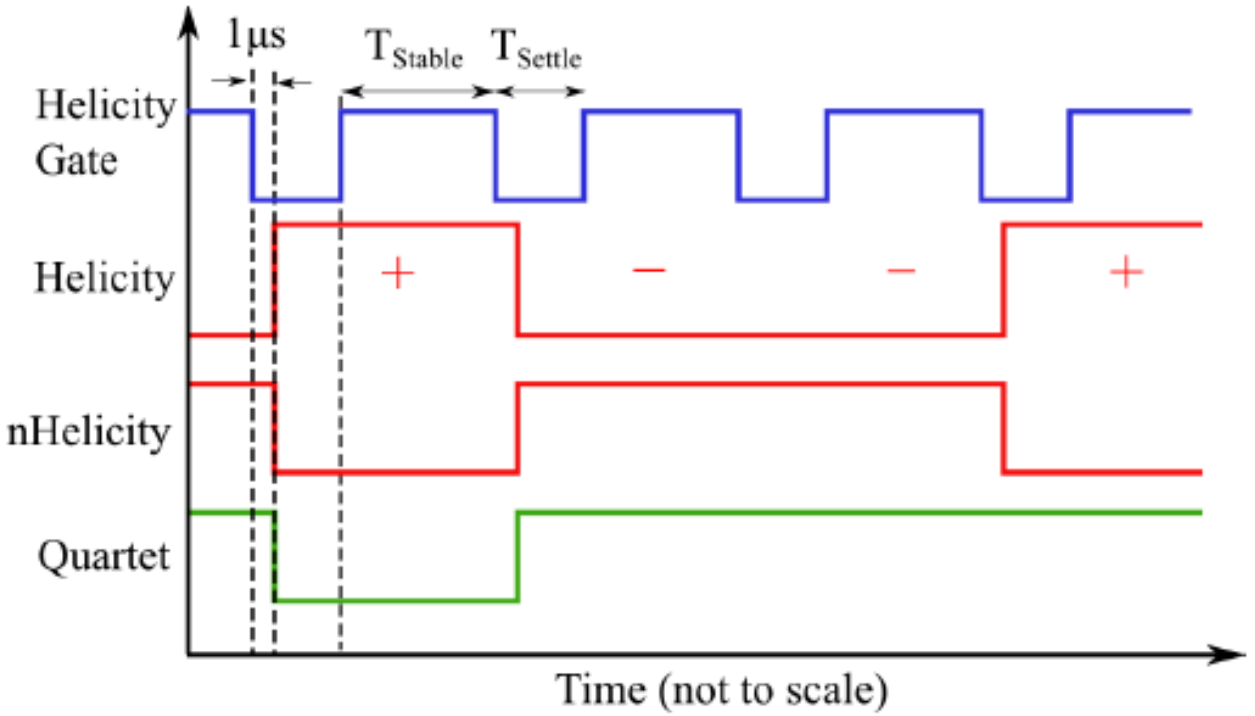
- Detector yields are integrated (sampled and summed) over each helicity state
- Raw asymmetries are formed from differences between positive and negative states
- Pattern asymmetries are histogrammed





Helicity windows and patterns

- The start of the stable window in the INJ DAQ will be used as the master trigger
  - If the signal latency feeding the INJ ADCs is not long enough for us to use the start of Tstable as the start, we will use a delayed copy of the start of the settle period as the master trigger
- Each ADC will start its integration when it receives its copy of the master trigger
- Possible helicity timing for 1919.938 Hz
  - 500.85 μs stable, 20 μs settle
  - 7364 14.71-MHz samples (1841/block)
  - Patterns of 64 windows span ~1/30 s
- Raster frequency example: ~23040 Hz & ~24960 Hz
  - Per window: 12 X cycles, 13 Y cycles, one pattern



Radiation hardness of electronics

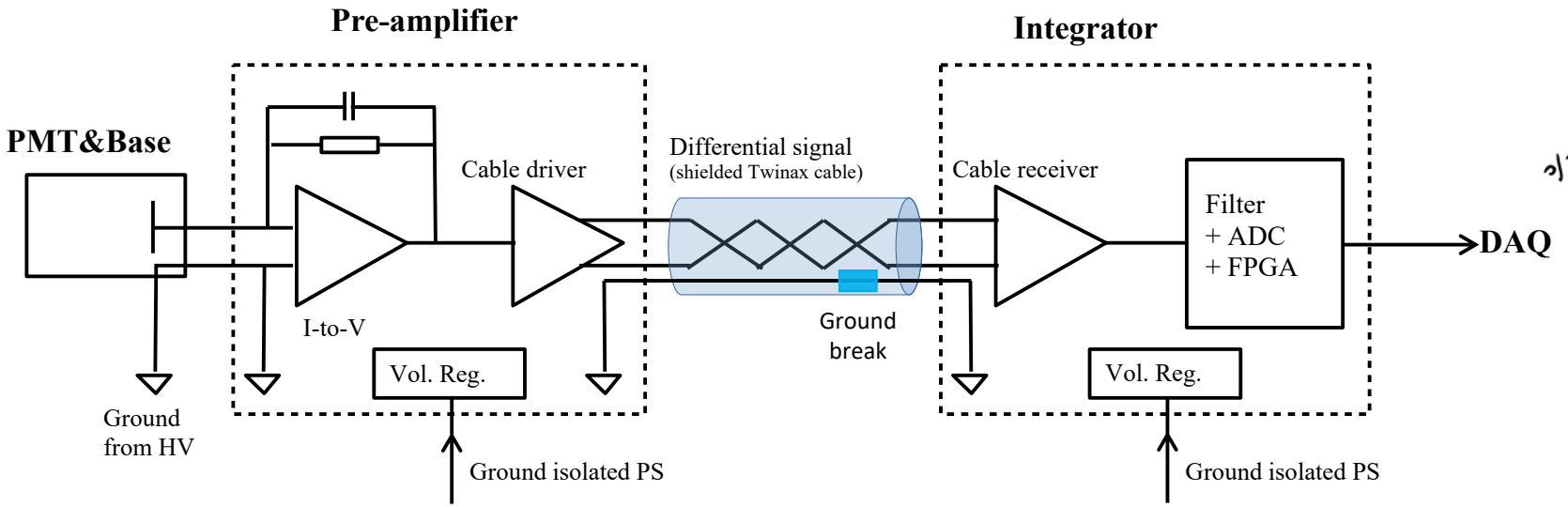
- PMT preamplifiers
  - Simulations with 5 cm of lead around the region of the PMT base and preamplifiers gave a dose estimate of 60 kRad for those components giving about factor 5 safety factor
  - Selected space-application grade components which are RHA (radiation hardness assured to >300 kRad by the manufacturer)
  - Conducted radiation hardness studies at Idaho

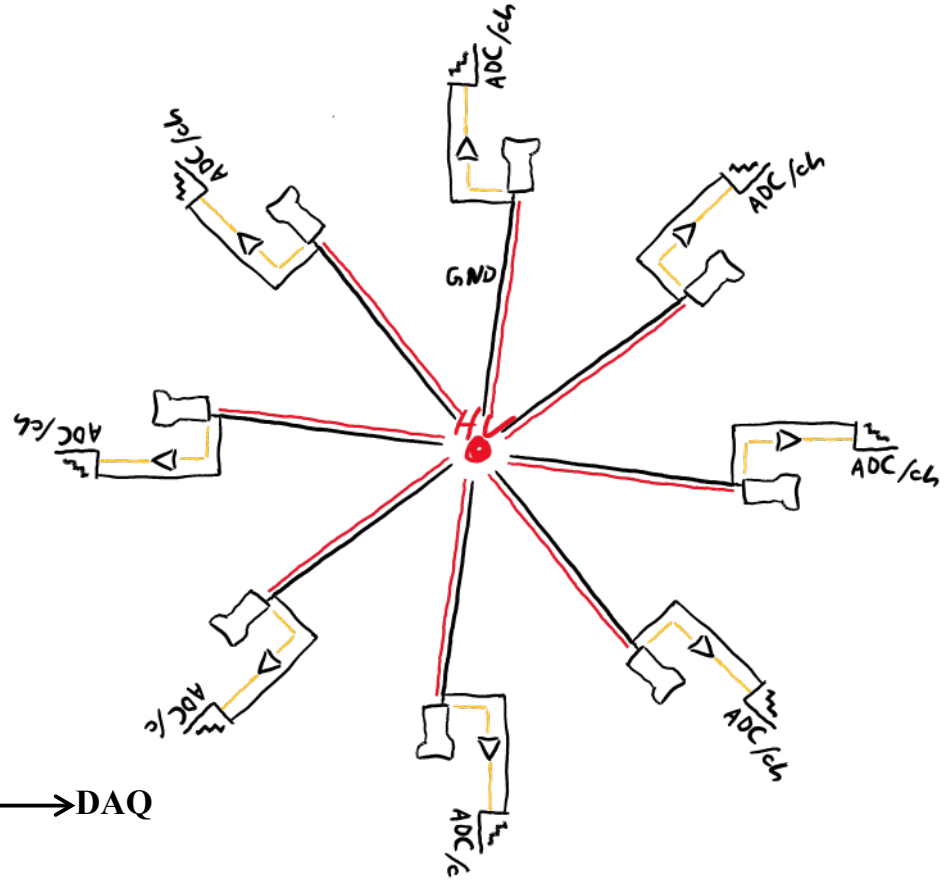
- Integrating ADC modules
  - These will be located in the upstream shielded electronics bunker, at a distance from the detectors and the target
  - The radiation environment has been simulated and is sufficiently low

Ground isolation plan

Integrating electronics detector ground isolation:

- ❑ Use ground-isolated power supplies for preamps and ADCs
- ❑ Ensure isolation between the PMTs in the mounting structure
- ❑ Use bike-spokes pattern formation to branch out to the detectors
- ❑ Implement separate ground path for each channel on ADC





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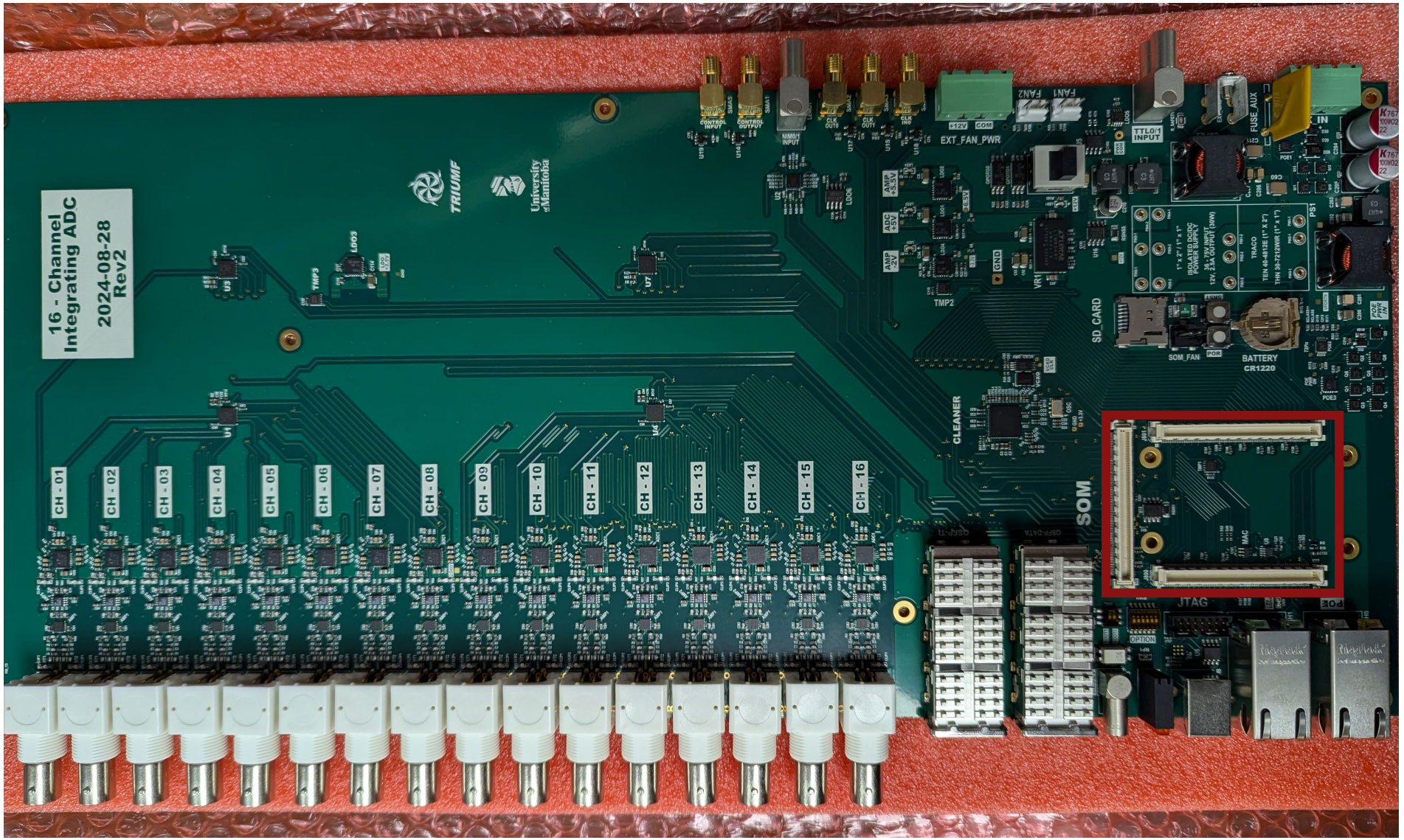
Integrating ADC, Revision 2



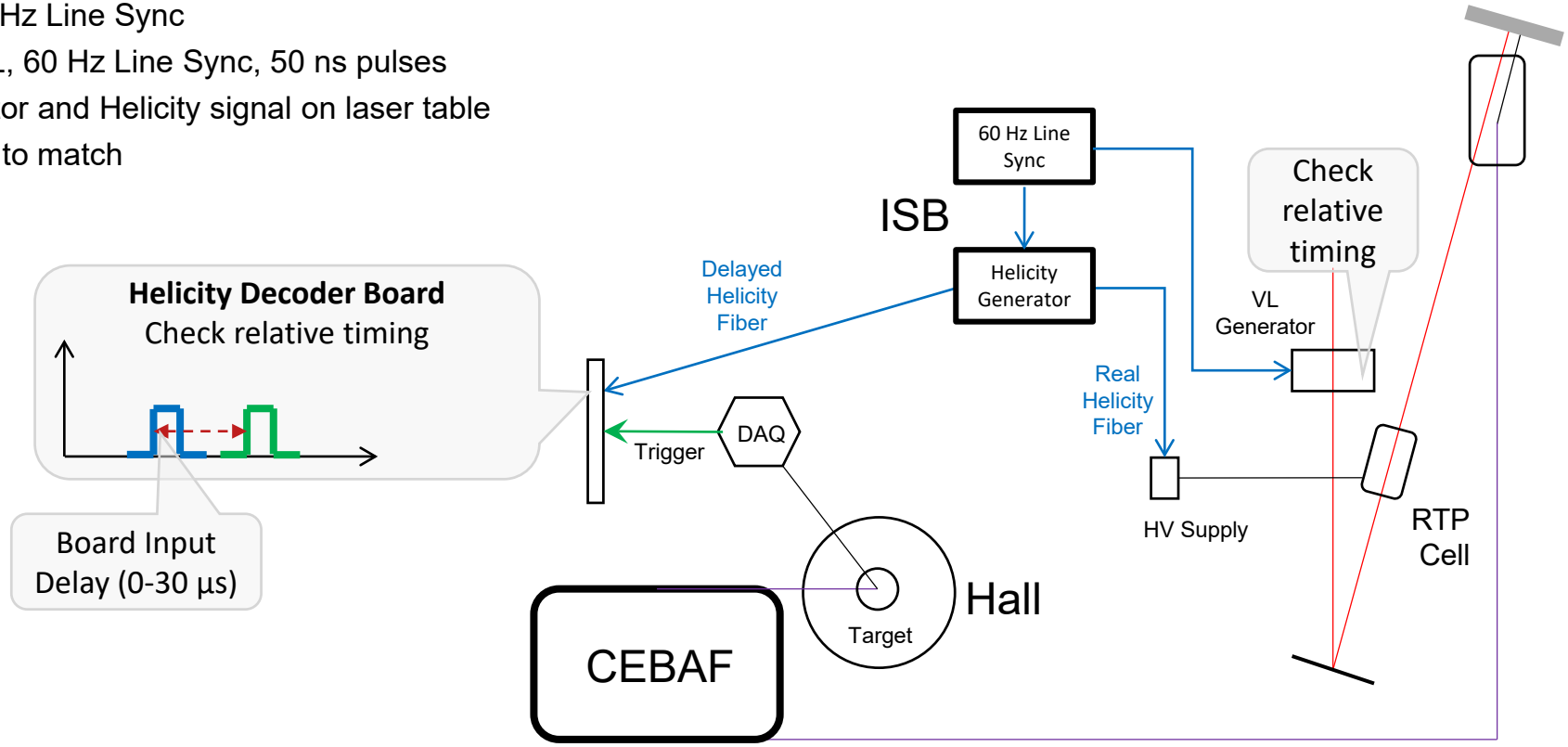
FPGA SoM connects here

Effect of gate time mismatch

- If an integrator gate is not properly aligned with the spin flip then the measured asymmetry will be deceased by a percentage of about twice the fractional misalignment
  - Alignment within 200ns out of 500μs (0.04% misalignment) would bound this effect ~0.08% decrease in the asymmetry
  - If the detector and beam current monitor integrals are not aligned with respect to each other, then a false asymmetry is introduced which is equal to the charge asymmetry times twice the timing mismatch percentage. This would appear as a detector non-linearity
- Using a narrow beam pulse at 60 Hz (tune mode) and the diagnostic waveforms from the detector and beam current monitor modules, we expect to be able to adjust the relative gate timing to 2 or 3 of the 15 MHz samples, which would be about 0.1-0.2μs

Adjusting for electron travel time

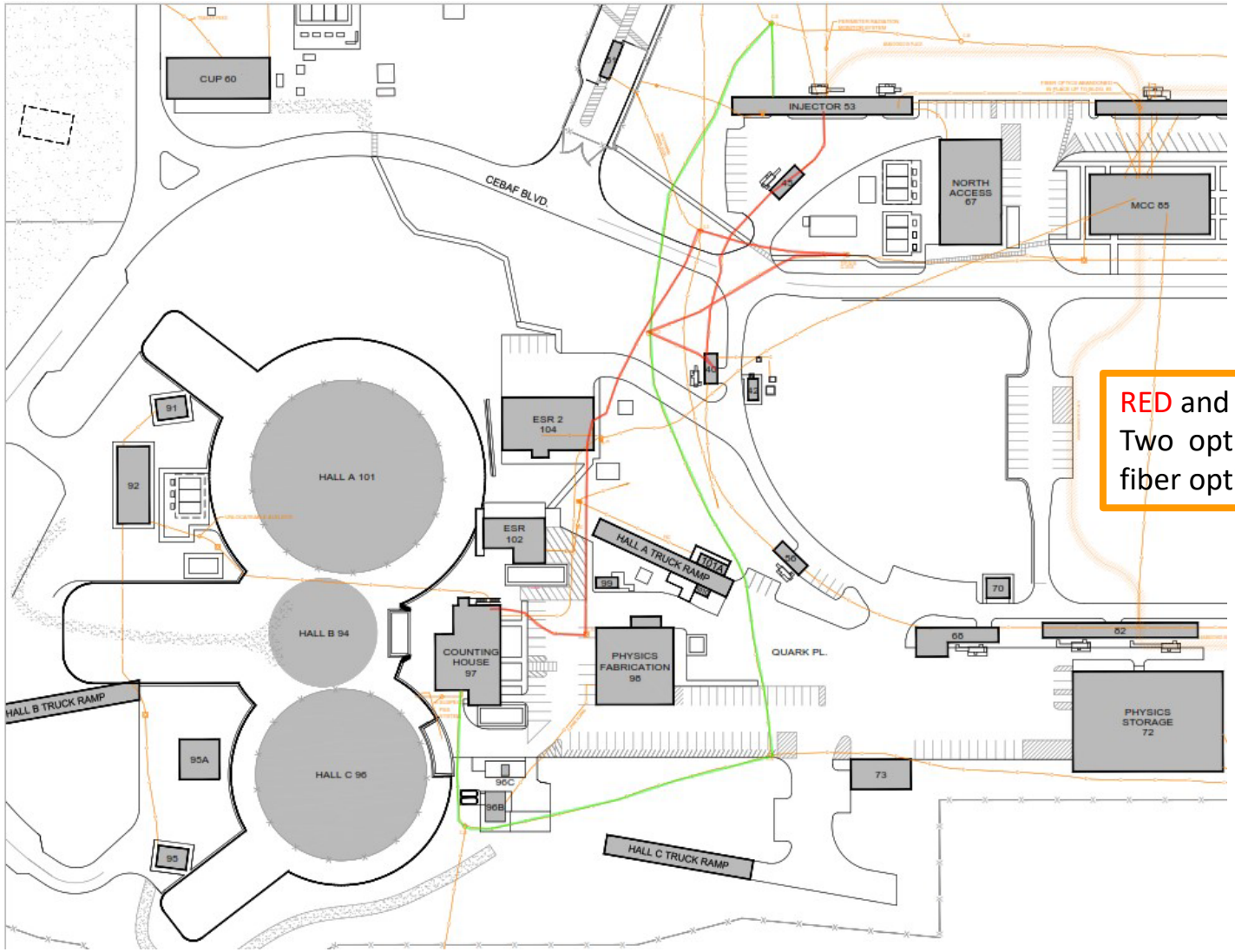
- With 10 μs T_Settle time, travel time from photocathode to Hall target becomes relevant. At 5th pass, travel time is ~21 μs. Helicity signal propagation to the hall is ~2.5 μs.
- How to set input time delays:
  - Helicity Board: 60 Hz Line Sync
  - Electron Beam: VL, 60 Hz Line Sync, 50 ns pulses
  - Check VL Generator and Helicity signal on laser table
  - Adjust gate timing to match



Slide courtesy of R. Suleiman

Fiber run for TI connection between ISB and Hall A

- JLAB Fiber Optic Site Plan:



RED and GREEN
Two options for routing fiber optic trunk

Multimode fiber trunk
144 fibers == 12 MTP
OM4 cable rating, 10Gbps
Armored jacket

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Bench testing of trigger distribution between ISB and TI-bridge in Hall A

TriggerGeneration (Timaster(slot#3))

↓ OpticFiber, SingleMode, 1500 ft

TriggerBridge (TI_bridge_supervisor (slot#6))

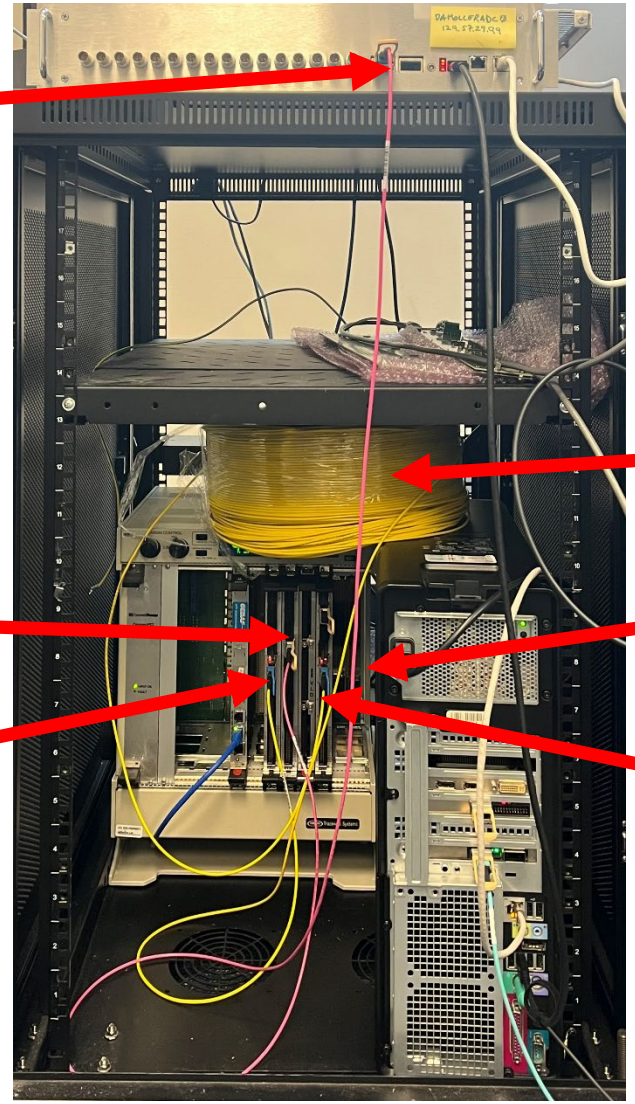
↓ fake_SD backplane

TD (TD (slot#4))

↓ OpticFiber, MultiMode, 6ft

Integrating ADC (TInode) in hallA

Integrating ADC (TInode) in the Injector Building (when the second ADC is available)



Picture and description, courtesy of W. Gu

Integration mode channels

- Detector array (280 total)
  - 224 Main detectors, 28 shower-max detectors, 28 pion detectors
- SAMs, LAMs, and beamline (226 channels)
  - SAMs: 8
  - LAMs and diffuse background monitors: 42 (14 LAM + 28 DBM)
  - Injector beamline: 96
  - Transport line and Hall beamline: 80 (PREX/CREX used 64; my count so far ~77 ch.)
    - Channels needed for beamline may be lower due to LBNL & JLab digital receivers
- Scanner (6+7 channels)
  - X/Y scanner: 2 PMTs + 2 position voltages (positions could go into a FADC or VQWK?)
  - Linear scanners: 4 PMTs + 4 position voltages
  - Reference voltage for positions
- Total: 512 channels → 32 16-channel modules
- HVMAPS & Digital BCM expect to connect into CODA in same way as ADCs

Data rate for integration mode

Production mode: 32 Integrator modules, ~130 MB/s

- 2048 bytes/module/window
  - 120 bytes/channel/window; 24 bytes per integral (sum, sum of squares, minimum, maximum, number of samples)
    - Full integral over the helicity window
    - Four sub-integrals in the “blocks” of the window
  - 8 bytes/channel/window timestamp
- Total data rate per module: ~4MB/s

Diagnostic mode: assume 1% of time, ~1.68 hrs per week

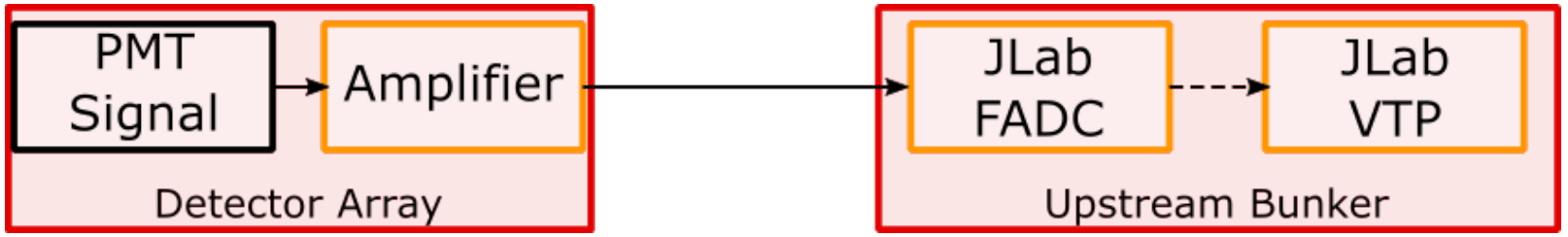
- Streaming all samples: 34 MB/s/channel
- Data estimate assumed capping the rate at ~1GB/s → allows 29 channels at once

- Data storage rate: ~450 GB/hr
  - Likely ~23 files of 20 GB
  - Each file would be ~2.5 minutes long
- Roughly 2 PB for a 30 week running period
- Total production data: ~7 PB
- Total diagnostic data: ~0.6 PB

Integration DAQ status and plans

- Integrating ADC: JLab has been testing with a pair of rev1 modules, and is about to receive two of the rev2 production modules
- Firmware for streaming mode has been in extensive use in test stands
- Firmware to do the sample accumulation exists for rev2 but most tests have used streaming mode; needs to be combined with changes in the rev1 firmware
- CODA readout controller can run on the module and get the streaming data from the FPGA
- Accumulation over the helicity window, TI triggering, and readout with CODA are all working, but in independent firmware versions and need to be pulled together
- MOLLER has a total of 40 integrating ADCs; 26 differential and 14 single-ended
  - Planned installation is 21 differential and 11 single-ended modules
  - As of May 30, 14 differential and 11 single-ended boards have completed testing at Manitoba

Counting mode data data acquisition channels



Amplifier inside PMT housing for thin quartz/shower max; use NIM amps in US bunker if needed for others

- Voltage and timing data: 336 ch. (21 FADC)
  - Detector array PMTs: 280 total; 224 thin quartz, 28 shower-max, 28 pion detectors
  - Trigger scintillators: 14; 2 each for 7 GEM sectors
  - Scanner PMTs: 6; 2 in X/Y scanner and 1 each in 4 linear scanners
  - Alternate trigger signals: 36; SAM- or LAM- signals? Diffuse background PMTs? Halo PMTs?
- Voltage data only: 23 ch. (2 FADC)
  - Beamline: Two cavity triplets and two stripline BPMs: 14 ch.
  - Raster readbacks: 2 ch.
  - Scanner position: 7; 2 for X/Y, 4 for linear scanners, 1 voltage reference
- GEM readout: APV25→MPD→VTP

MOLLER Counting DAQ JLab – Summary of Activities and Plans (S. Malace)

MOLLER Counting DAQ in Test Lab: MOLLER Pion Detector and Scintillator Tests

One VXS crate with one FADC (more can be added, if needed) and one VTP to form VTP-based triggers for dual purpose (CPU, SD, TI as well):

→ Characterization of Single Photoelectron (SPE) response of the Pion Detector PMTs

→ Cosmic rays tests of the Pion detector bars once they are assembled

This is the same setup that S.M. used in TEDF last year to characterize the Pion detector PMT of choice and run cosmic rays tests of the Pion detector prototype

As of recently the setup has been used for MOLLER scintillator prototype tests and this will continue as needed in parallel with the Pion detector tests (Tasneem and Zhongling, with support from Simona)

https://logbooks.jlab.org/entry/4371422
https://logbooks.jlab.org/entry/4374404
https://logbooks.jlab.org/entry/4386092

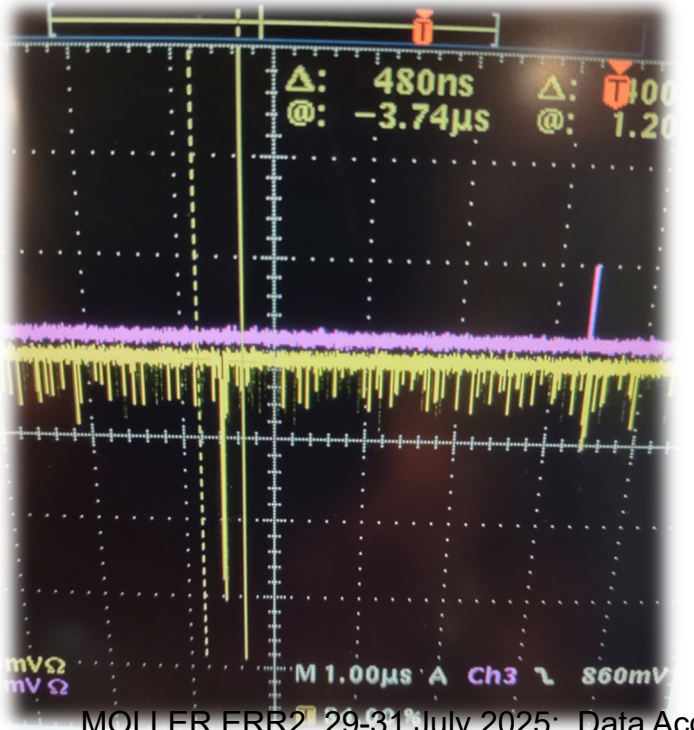
MOLLER Counting DAQ JLab – Summary of Activities and Plans (S. Malace)

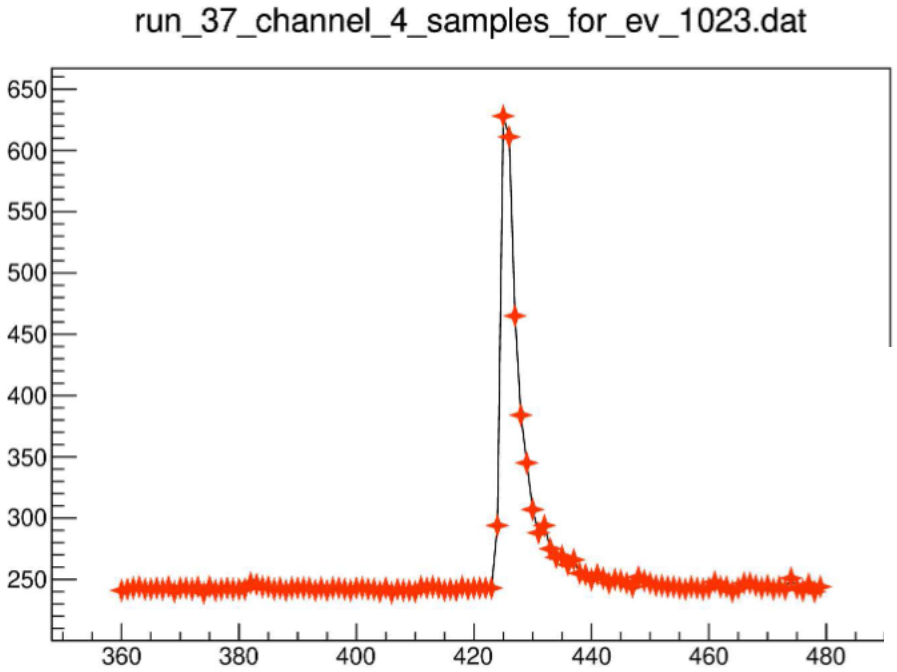
MOLLER Counting DAQ in Test Lab: MOLLER Pion Detector and Scintillator Tests

Trigger OUT signal from the SD card (pink)

MOLLER scintillator pulse (yellow)

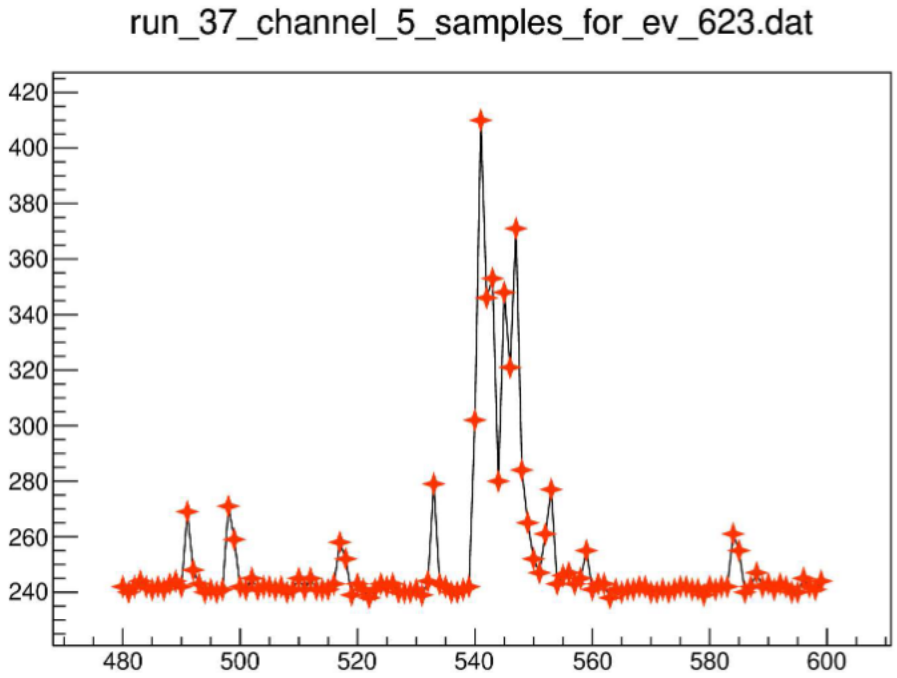
Vertical bars: FADC sampling window (120 samples)





Waveform from one of the 4 scintillator paddles that are used to form for a 4-fold coincidence trigger ()

Example of MOLLER scintillator response when an external trigger is formed by the passage of a cosmic ray through 4 scintillator trigger paddles



MOLLER Counting DAQ JLab – Summary of Activities and Plans (S. Malace)

MOLLER Counting DAQ in ESB: The MOLLER experiment Counting DAQ setup to be eventually moved in Hall A

Two VXS crates with v2 and v3 FADC250s, VTPs to form VTP-based triggers, CPUs, SDs, Tis for dual purpose:

→ Testing of the MOLLER counting DAQ VTP trigger with pulsers

→ Testing of the v3 FDAC250s

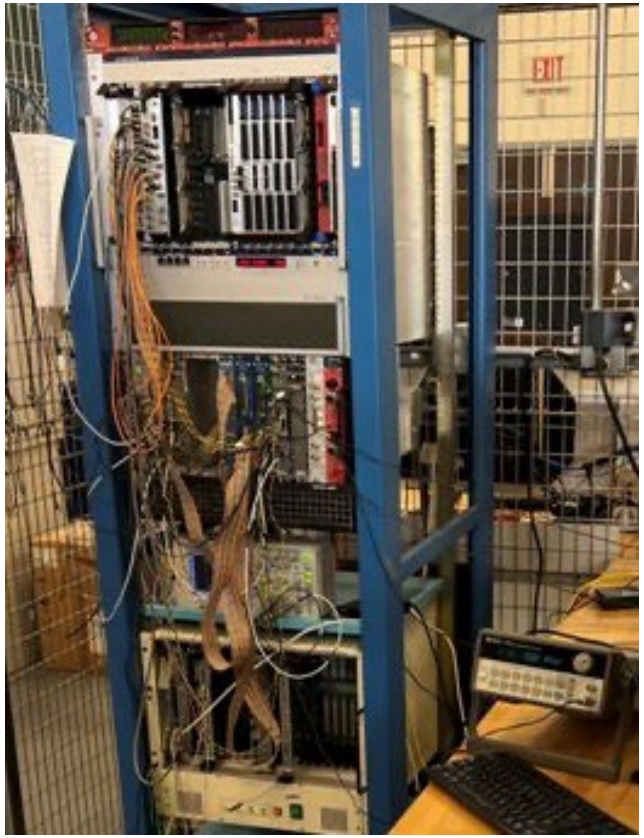
V3 FADC250s have been tested initially by the JLab Fast Electronics group for QA acceptance

As of now the firmware that allows the v3 FADCs to interface with the VTPs for VTP trigger formation is in the works

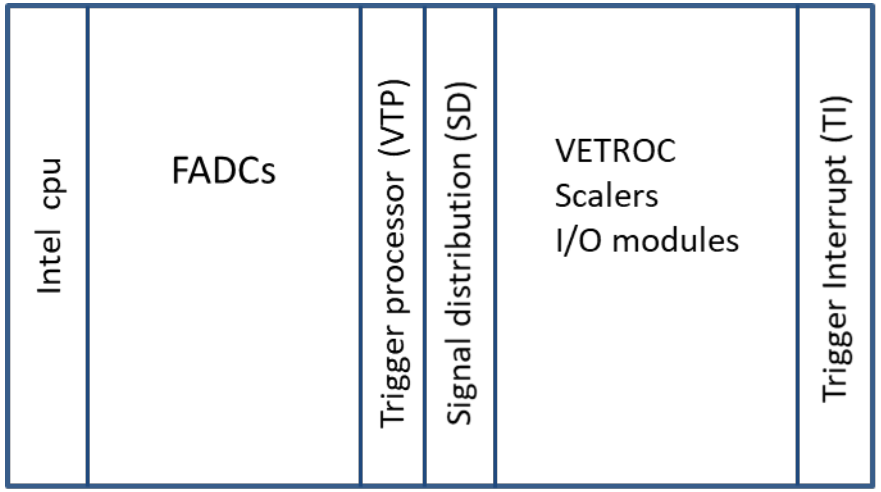
In the ESB the v3 FADC250s will be tested initially against the v2 FADCs for pulse processing

Once the new firmware is available the v3 FADC250s will be used to vet the MOLLER counting DAQ trigger

Counting Mode Test Stand



- Test stand in TestLab used for common development of counting mode, Compton polarimeter, and Moller polarimeter DAQ systems
  - DAQ designs share same concept: FPGA in VTP collects data from front-end (FADCs or VETROC) to form event triggers
- Development objective for counting mode: VTP firmware to trigger on FADCs of single elements (quartz tiles) or two-channel coincidences (trigger scintillator)



Counting DAQ rates & data size

- Total Moller rate: 135 GHz@65 uA → ~300 MHz/sector/uA
  - 100nA: 30MHz/sector, ~7.5 hits/sector/256ns
- GEM samples: 6 25-ns sample
  - Full data rate: 18.4Gb/s (2.3GB/s)
  - 0.614 Gb/s from each MPD
  - Zero suppression in VTP with 30% occupancy would give 690MB/s (5520Mbps) from VTP
    - Occupancy based on 5 hits/GEM layer & 8 strips per hit is ~3%
- FADC trigger window range: 256ns (64 samples)
  - FADC raw mode data rate at 5kHz: 264 MB/s
    - 336 FADC channels * (64 samples * 2 bytes/sample + 4 bytes for channel) → 222 MB/s
    - Estimate 20 particles with 5 detectors hit (2 scint, 1 quartz, 1 showermax, & 1 pion) in each sector per trigger; pulse parameter data (3 longwords?) would give ~42 MB/s
  - One crate would have 14 modules: ~1408Mb/s from that crate; should readout through VTP
- Total data rate at 5kHz with full raw FADC readout & 30% occupancy in GEMs: 954MB/s

Recommendations from the PDR and actions taken

- Continue plans for reviews of circuit board designs with Jefferson Lab staff before release of production versions.
  - JLab staff have been actively involved in development of the integrating ADC module; W. Gu conducted a review for FEG of the DAQ plans
- Update/verify existing electrical/grounding system drawings for Hall A to include new equipment for MOLLER detector and magnet apparatus.
  - The collaboration's Grounding task force has a draft grounding plan that is being evaluated by JLab electrical safety experts
- Carefully review the requirements for new fiber optic cables from the Injector Service Building (ISB) to the Hall A electronics bunker locations and create an installation plan.
  - The plan for the ISB-to-CHA has been complete, and installation is expected in the current SAD
- Make progress on the prototyping of the Integration/readout board a priority. The more time it can be tested and integrated into the CODA framework the easier it will be to flush out all potential DAQ and timing issues.
  - Development of the CODA routines using the prototype ADC module has started

Response to FDR committee about experience with GEMs in SBS

We want to make sure the DAQ talks tomorrow cover issues experienced in SBS with readout used for their GEM system.

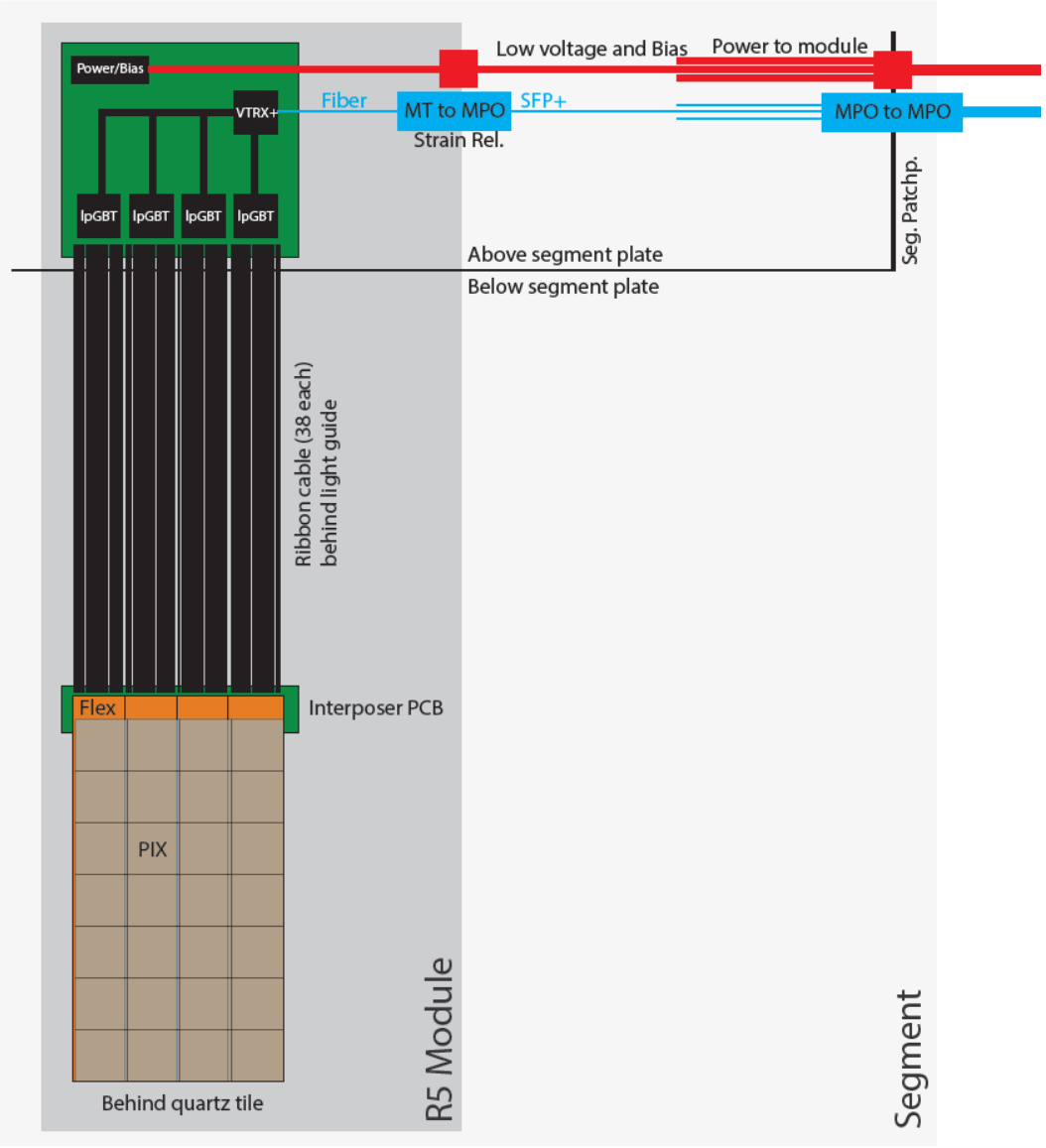
- SBS uses GEMs in both BB and SBS using the APV→MPD→VTP readout chain
- A lot of the stability issues at the start of GMn were resolved with various firmware updates both to the VTP and MPDs.
- The big limitation, as seen by SBS, is the transfer of data from MPDs to VTPs and from VTPs to network
- Remaining instability issues now generally occur for various reasons when an APV misses a trigger.
  - Bryan and Ben have added diagnostics to tell which APV or which MPD is causing the problem, and there are procedures to power cycle the MPD crates, VTP crates, or the low voltage to the APV card. This usually can fix any APV issue that is not a physical cabling or disconnect problem, and they continue to gain experience with this.
  - They also have configurations in which problematic APVs can be disabled
- The BB GEMs occasionally cause DAQ issues at the start of run in our current running (just needs a reset most of the time), and the SBS GEMs cause problems at about the same rate x2-3 or so due to the larger number of channels
  - This is roughly 1 or 2 issues in 1-2 shift days for the BB GEMs
- The INFN GEM layers are the only ones that are still having issues right now, but these have a different design than the other layers, and they think the problem has something to do with the low voltage configuration

Response to FDR committee about experience with GEMs in SBS, pt2

- MPD data transfer links are 1.25 Gb/s and VTP output link is 10 Gb/s
- MOLLER (280 APV, 28 MPD) is similar in size to BB (328 APV, 24 MPD) but expects lower data rates
  - Most of SBS MPD cards readout 15 APV, but MOLLER will have 10 APV per MPD, so the data rate from a typical MPD will be 2/3 of SBS's at the same rate and number of samples
  - In order to saturate the VTP 10GbE link after zero suppression with 5kHz event rate, MOLLER would need to have GEM occupancies of ~58%; we expect 5-10% at 100nA, and can reduce beam current or prescale triggers if needed
- MOLLER will benefit from the continuing development of the APV→MPD→VTP readout chain during SBS
- MOLLER's design already incorporates one lesson from SBS: using more MPDs than the minimum decreases transfer time by having more links

HVMAPS

- Each Ring-5 tile would have 28 HVMAPS chips
- Readout from HVMAPS done via low power gigabit transceiver (lpGBT) SER/DES chip and the VTRx optical transceiver
  - One lpGBT supports 7 HVMAPS; four lpGBT supported by one VTRx
  - VTRx output is SFP+ fiber
- Data collected by FPGA accelerator PCIe cards (BittWare XUP-VV8)
  - Server chassis will have a TI-PCIe to allow CODA integration
- HVMAPS will be part of counting mode DAQ; will be operated independently during integration mode running



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HVMAPS Operation goals

Counting mode

- Pixels are self triggered, and send their hit data and timestamp over the fiber connection
- FPGA on Arisa switch uses timestamps to associate HVMAPS pixel hits to triggered event
- Fairly loose requirement to match timestamps to trigger due to 25 ns time binning on GEMs
- Pixel hit data is send to CODA data stream to allow combined analysis with GEM tracks

Integrating mode

- Run as independent data stream to generate an occupancy map
- HVMAPS are run in a triggered mode, to just record being hit within a narrow trigger window (~10 ns)
- All hit pixels are read over the fiber and accumulated to form a 2D occupancy map
- Likely also store a small fraction of the data from individual trigger windows
- Estimated stored data rate of 11 MB/s

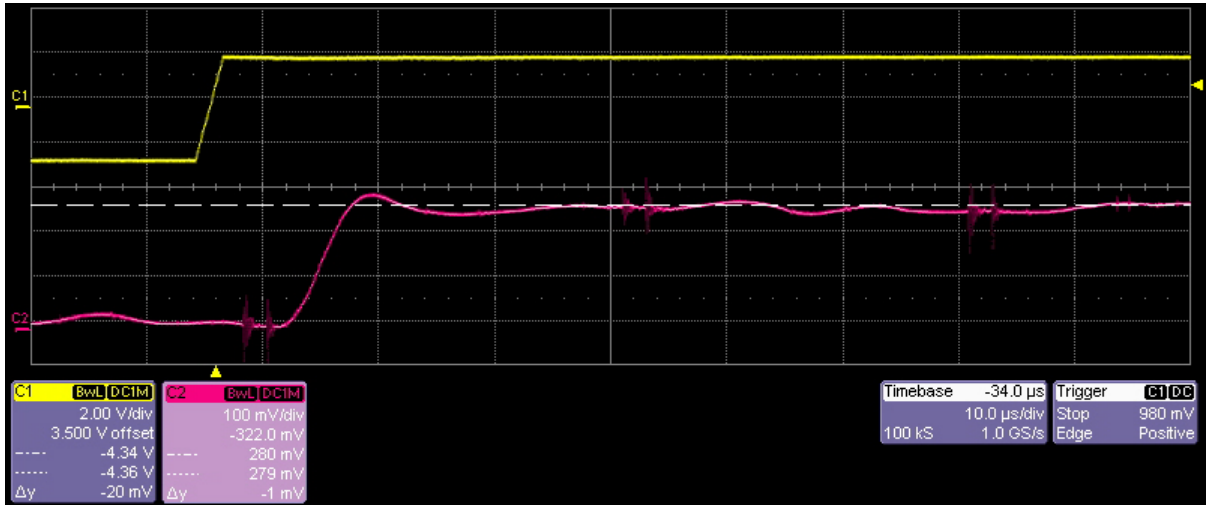
HVMAPS data rate estimate

- In counting mode, all hit data will be streamed to the FPGA server
  - Data rate per ring 5 tile at 100 nA: 320 Mb/s (40 MB/s)
    - Chips per ring 5 tile: 28
    - Data rate per chip: 11.2 Mb/s
      - Hit rate per chip at 100 nA in center of the ring 5 open sector: 280 kHz
        - Hit rate per chip at 65 μA beam current in center of the ring 5 open sector: 180 MHz
      - Row and column address of hit pixel and time stamp: 40 bits
  - The lpGBTs and VTRX+ chips support 1.28 Gb/s on each lpGBT (which serves 7 chips)
  - Only hits corresponding to CODA events will be recorded; even using a very loose 1 μs window at 5 kHz event rate would give suppression to 0.5% of raw rate
    - Recorded data rate from HVMAPS: (84 tiles * 40 MB/s * 0.5%) → 17 MB/s or lower
- In integrating mode, would gate the HVMAPS for ~100 ns with a periodic trigger
  - The lpGBT links would saturate near 200 kHz gate rate
    - Data for one lpGBT in 100ns gate at 65 μA: (18 hits * 40 bits * 7 chips) → 5 kb/gate/lpGBT
  - Actual trigger rate for HVMAPS would be adjusted to give the data rate we want
    - Data per 100ns gate at 65 μA: (18 hits * 40 bits * 28 chips * 84 tiles) → 1.7 Mb/gate
    - FPGA server 10GbE output would saturate at ~5000 Hz gate rate

Bandwidth and latency considerations for beamline readout

- We have sent a BPM and BCM requirements document to N. Rider
  - Highlighted the bandwidth and timing requirements to match with the detector signals

Bench test of BCM digital receiver, showing latency.
Courtesy of J. Musson



- JLab SEE electronics
  - Bandwidth of analog output signals is ~30kHz
- JLab digital receivers
  - Digital sample rate is 1Msps, allowing a maximum bandwidth of 500 kHz
  - Analog output (18-bit DAC) signals have a filter with effective bandwidth of 100-200 kHz
- For both the JLab SEE and digital receivers, the analog outputs have a few µs latency compared to the inputs. We will allow for this by adjusting the integrating ADC gate timing.

Beam monitor readouts

- All JLab BCM and BPM receivers have analog outputs which can go to ADCs
- Direct digital readout would improve resolution; development underway for Hall A/C experiments

Planned Readout of Digital Data for Beam Monitors

https://userweb.jlab.org/~rom/digibcm

J. Musson's electronics

CAEN V2495 PLU

Beam Monitor Electronics

beam current (BCM) or beam position (BPM) Digital data

Fiber

Electronics that sums the data in each integration window and can be read out by the DAQ

Integration gate
4 usec to ~1 hour

John Musson
Chad Seaton
Bob Michaels
Randall McClellan (initial version)

- UC Berkeley and LBNL are developing a digital BCM receiver
  - The input bandwidth is closer to the integrated PMT channels
  - Trigger Interface connection and readout would be done through QSFP as for the integrating ADCs

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Throughput testing of japan-MOLLER

- We had run tests using analysis of japan-MOLLER mock-data on the “aonl1” machine (the newest of the CHA cluster)
  - Processing a mock-data file with 488 MOLLER ADC channels, producing all histograms and TTrees, and doing regression of the detector channels against the five primary beam parameters, throughput was about 4-5 milliseconds per event (i.e 10 times slower than data rate)
    - This is about 5 times faster than I had expected by scaling from the Qweak performance
  - Contrary to the experience in Qweak, we could run up to 10 simultaneous jobs on that machine without significant impact on the processing time
    - We can run more jobs per machine, so need fewer machines
- If this throughput continues to hold, and if we process each 2.5 minute file-split as soon as it closes, fully processed results would be available with a lag of about a half-hour
- Note that we need to validate the this performance using using the real MOLLER-ADC data stream, and adding processing algorithms may increase the time per event