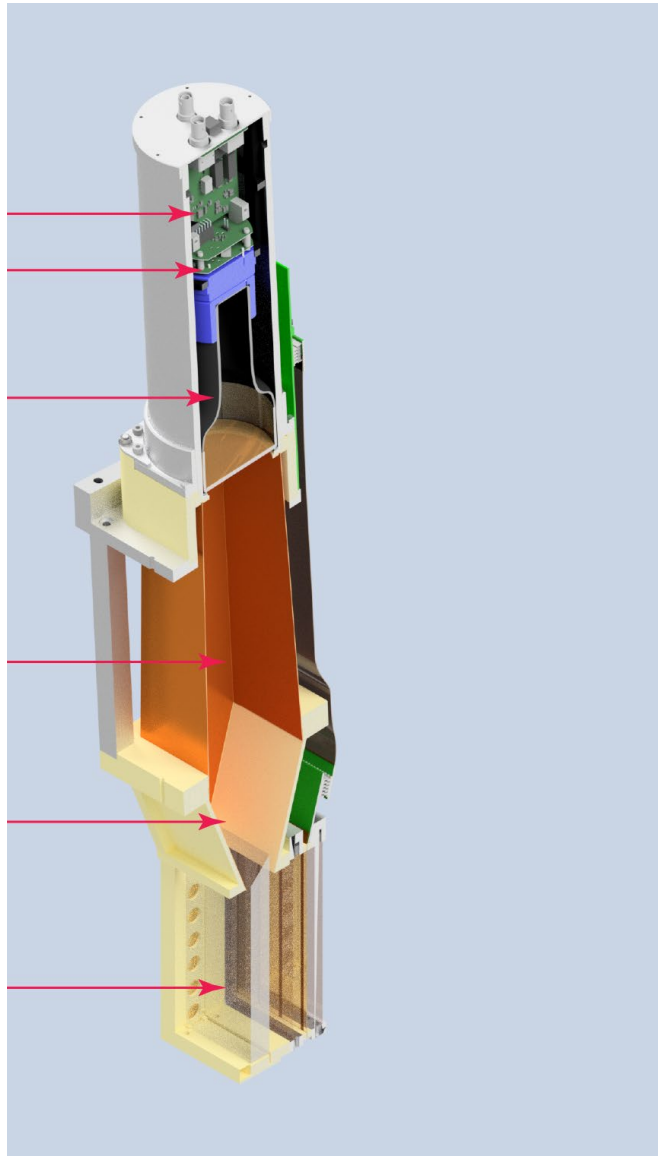
Ring 5 HVMAPS

MOLLER Collaboration Meeting
May 2023

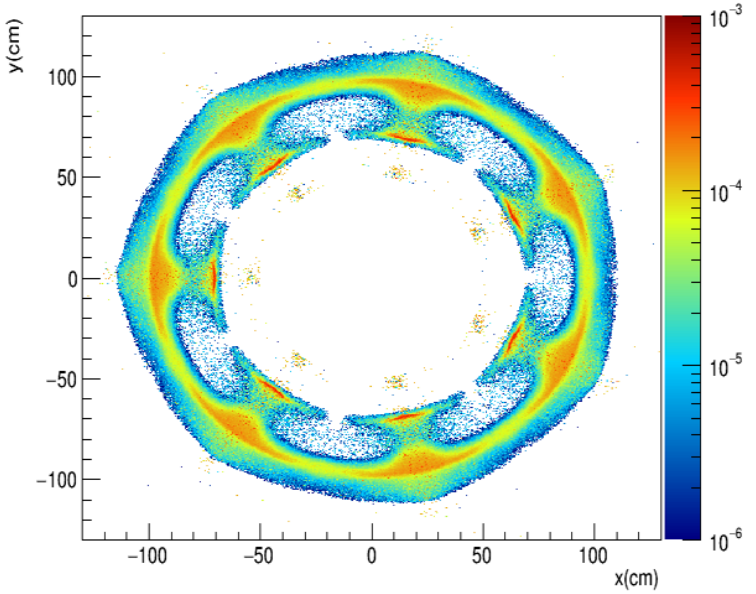
Michael Gericke

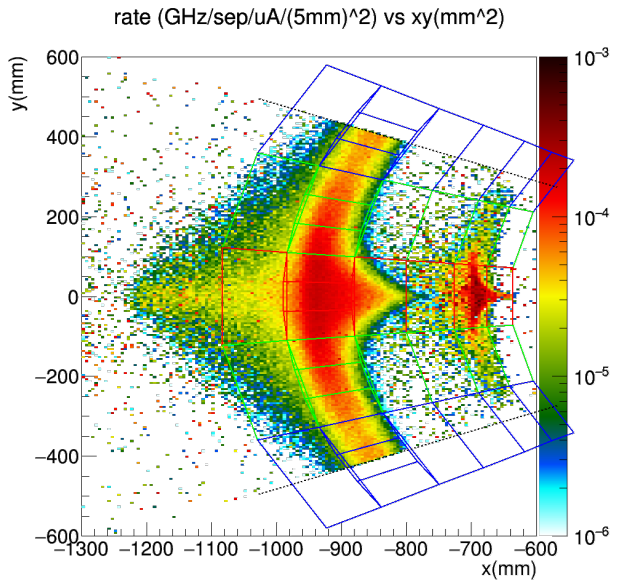
- Motivation
- Operational principle
- Readout setup
- Cabling Plans
- Housing/Mounting/Cooling Kristofer Isaak



Motivation:

- The precise and correct measurement of the asymmetries depends on the correct event separation in the detector tiles, as indicated by the ideal event profile.
- Changes in beam properties and magnetic field non-uniformities lead to shifts in the event profile and change the measured event type share in a given tile.
- If these changes are helicity correlated this can lead to a false or incorrectly extracted asymmetry.
- Careful periodic tracking measurements with the GEM detectors event mode will verify the kinematics and the associated event profile at low current.
- The HVMAPS can be used as another tracking plane behind the ring 5 detectors at these lower currents, together with the GEM detectors.
- They could provide a measurement of background events created between the GEMS and ring 5.
- They can verify the profile at high beam currents due to their radiation hardness and high event processing speed (at fully beam current they have to be gated).

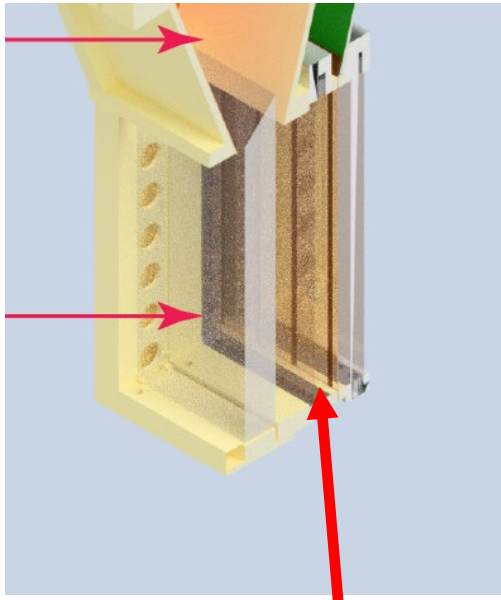


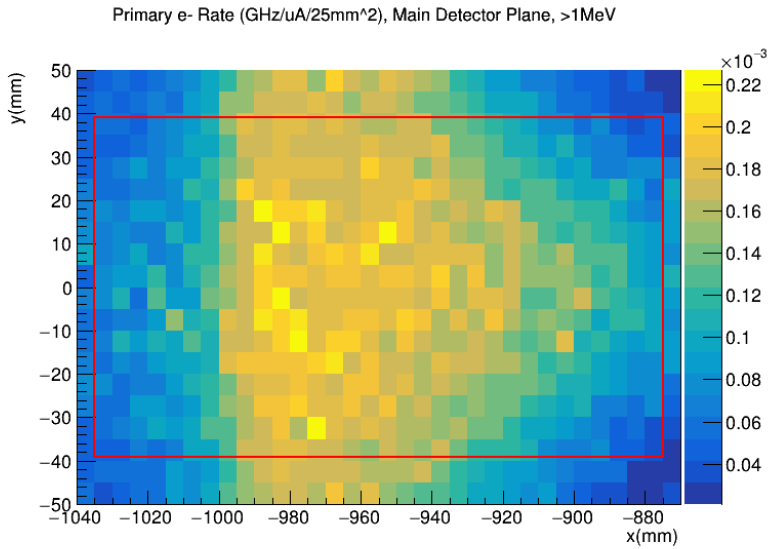


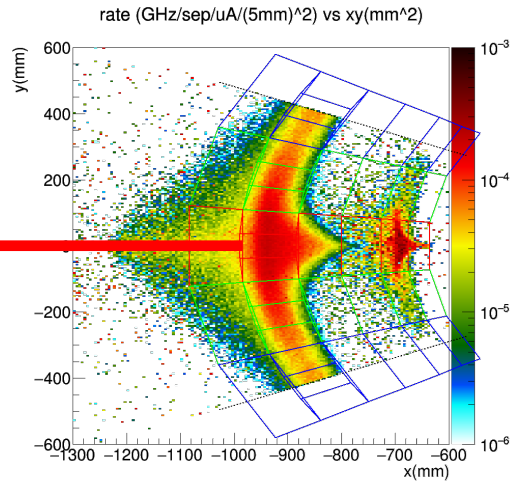
Motivation:

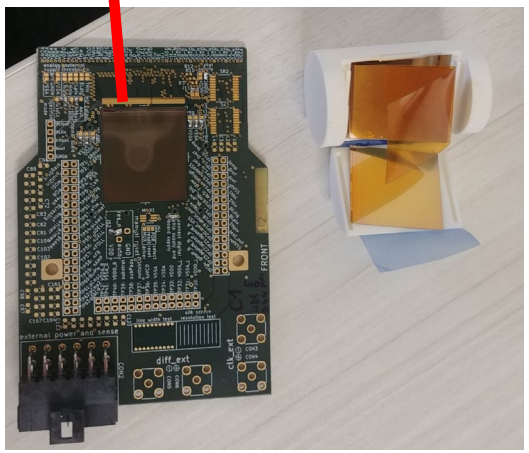
CFI funded parts

1. 2352 Pixel chips: 28 per ring 5 tile
2. Mounting structure (including flex-print)
3. Cooling equipment
4. Front-end boards with lpGBT and VTRX+ (CERN)
5. Cabling
6. Power supplies
7. FPGA boards



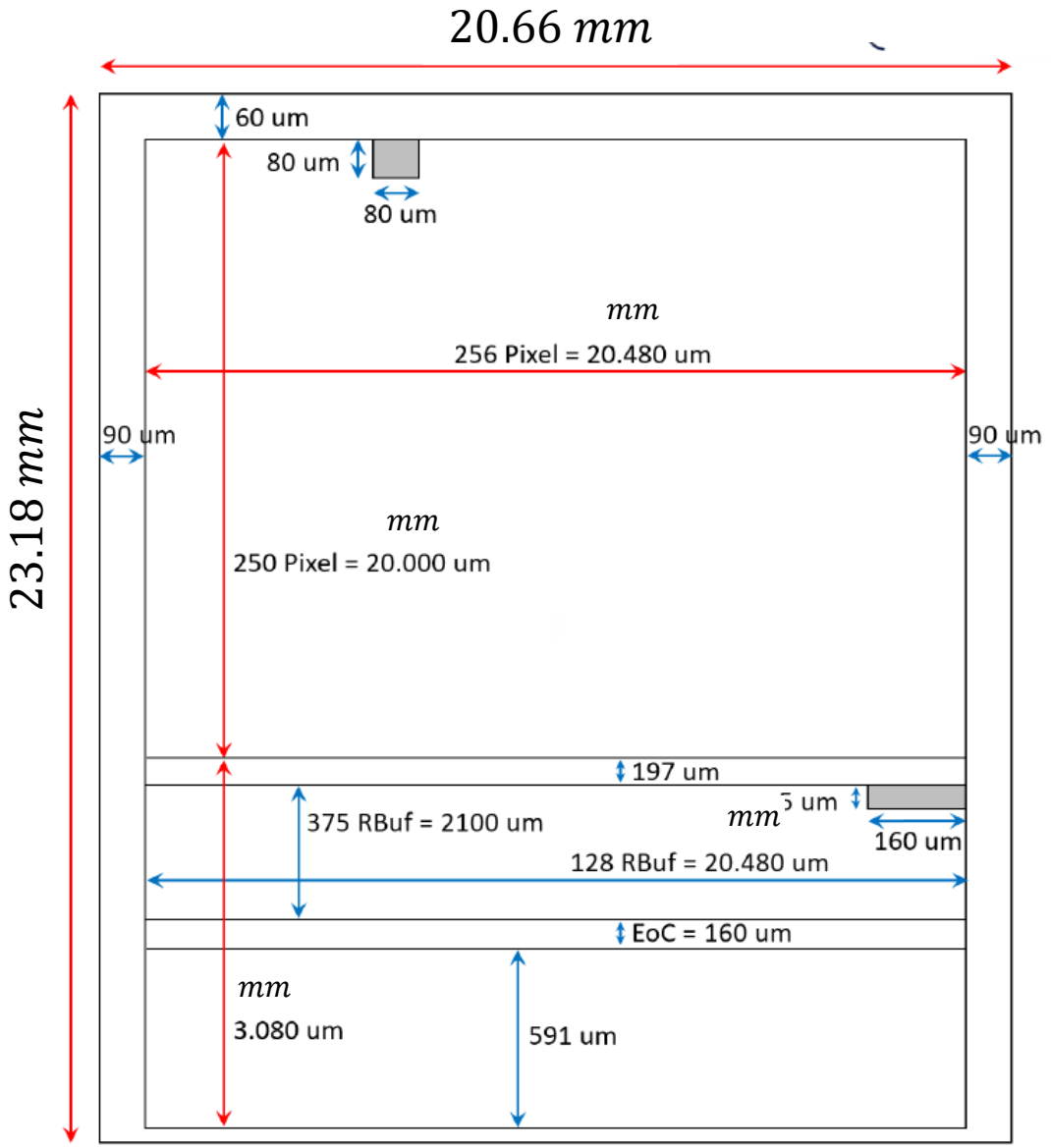


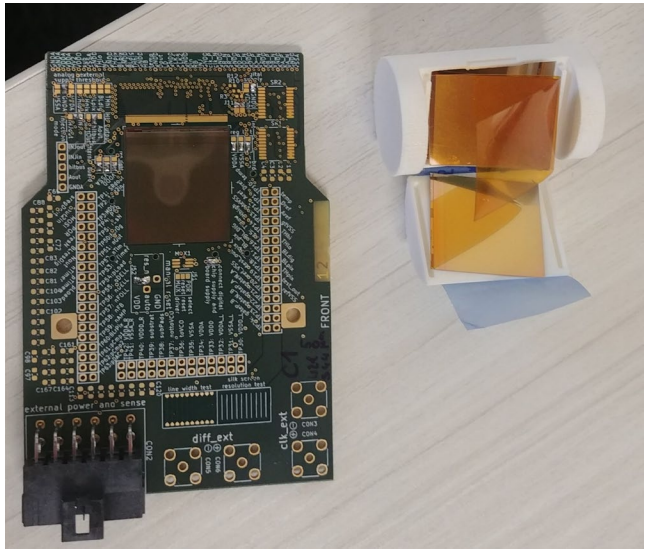




Operational principle:

- The final size of the individual chips is ~20 mm by 23 mm
- 64000 pixels per chip ($80\ \mu m \times 80\ \mu m$)
- Several of them are to be combined to form a plane of whatever size is needed

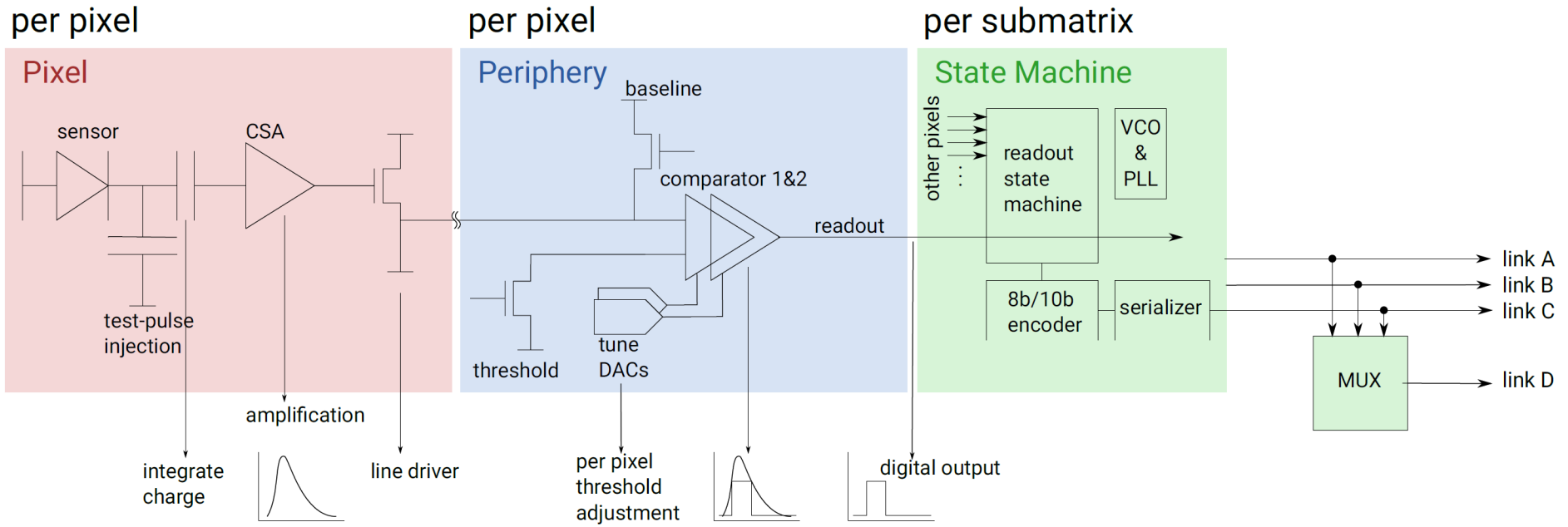




Summary of HV-MAPS operation (with figures by Heiko Augustin, Alena Weber, and Andre' Schoening – U. Heidelberg)

- There are three distinct areas of the chip:

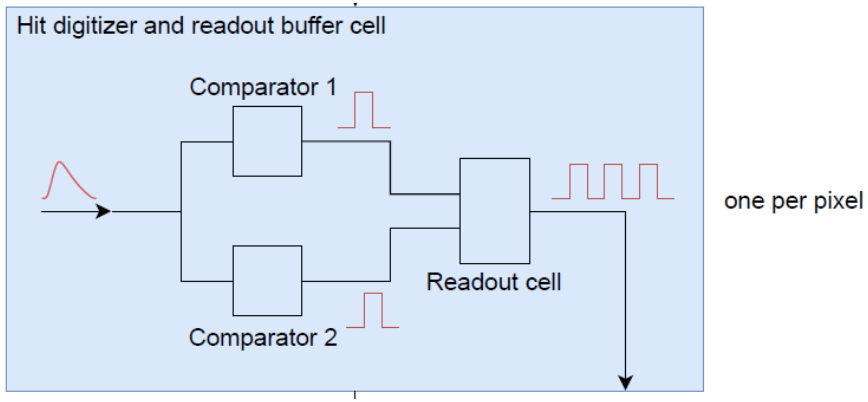
  1. The pixel area, in which each of the 64000 pixels include an amplifier and a line driver to connect the pixel to the periphery
  2. The mirror pixel area at the chip periphery, which includes two tunable ToT comparators
  3. Three state machines at the chip periphery and a mux for data transfer

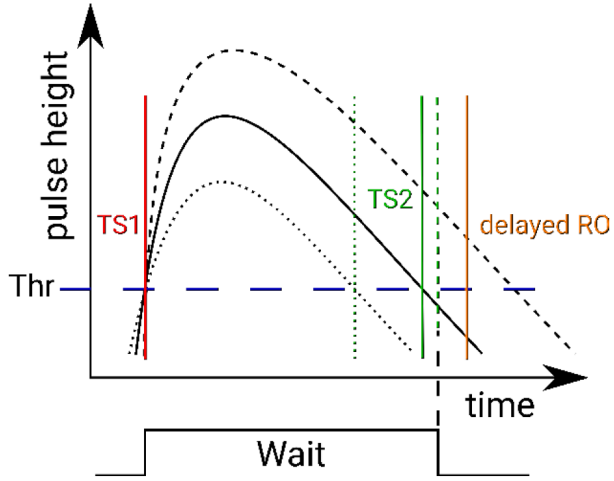


Summary of HV-MAPS operation

- Signal digitization and time stamp generation:

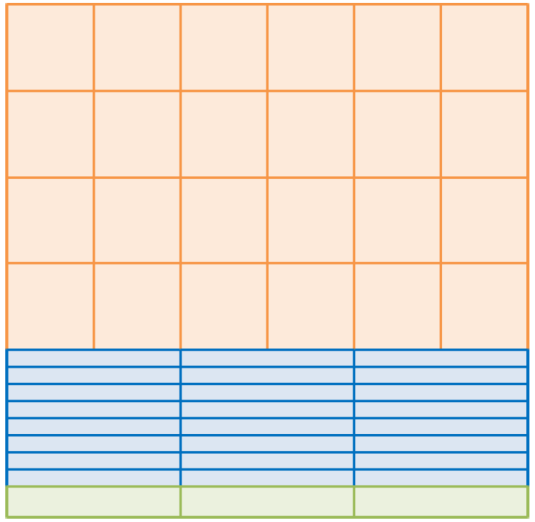
1. Each pixel drives the amplified hit signal to a dedicated readout buffer at the chip periphery
2. The two comparators for each pixel are part of the readout buffer circuitry
3. The readout buffer generates two timestamps. The first one sets the hit latch. The second one establishes the ToT proportional to the collected charge and reduces time-walk effects.
4. The buffer stores an 8b pixel row address and the two timestamps (TS1 = 11b and TS2 = 5b)

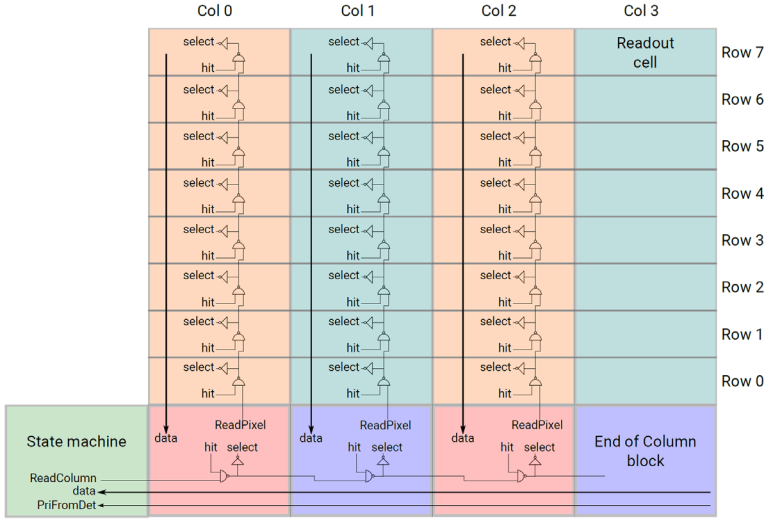




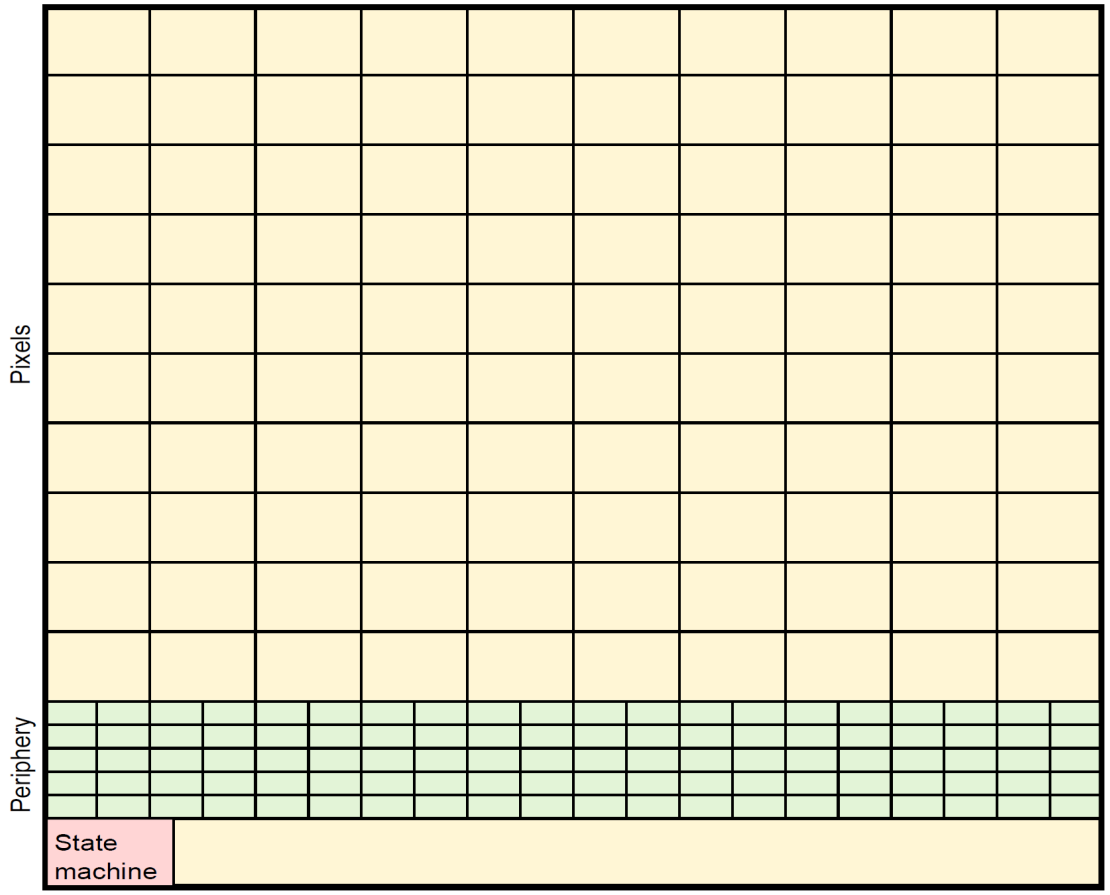
Summary of HV-MAPS operation

- Chip event readout organization:
  1. The chip is readout in column-drain and row readout sequence. There are 250 rows and 256 columns
  2. Pixels buffers with hits are transferred to an EoC (End of Column) cell, selected by a priority logic.
  3. If a pixel buffer hit state is transferred to the corresponding EoC, the buffer is cleared and the pixel is sensitive to new hits again.
  4. The EOC contains an 8b column address and collects the full 32b hit information
  5. The priority chain within a column is based on pixel position and hit time
  6. The state machine generates signals to transfer the pixel hit information to the EoC and transfer the 32 bit EoC data to the serializer
  7. The 32b data words are byte serialized and 8b/10b encoded





Summary of HV-MAPS operation

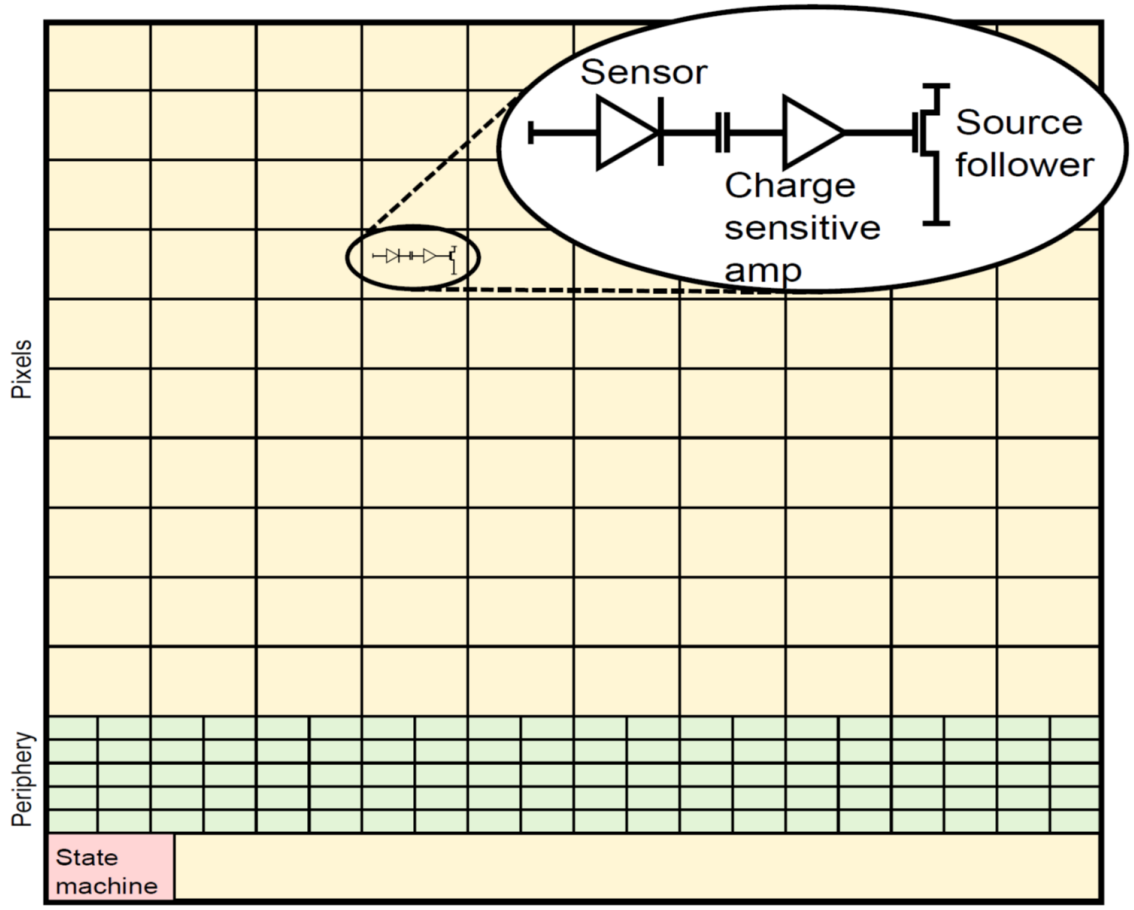


Pixel area

Pixel buffer area

Readout logic

Summary of HV-MAPS operation

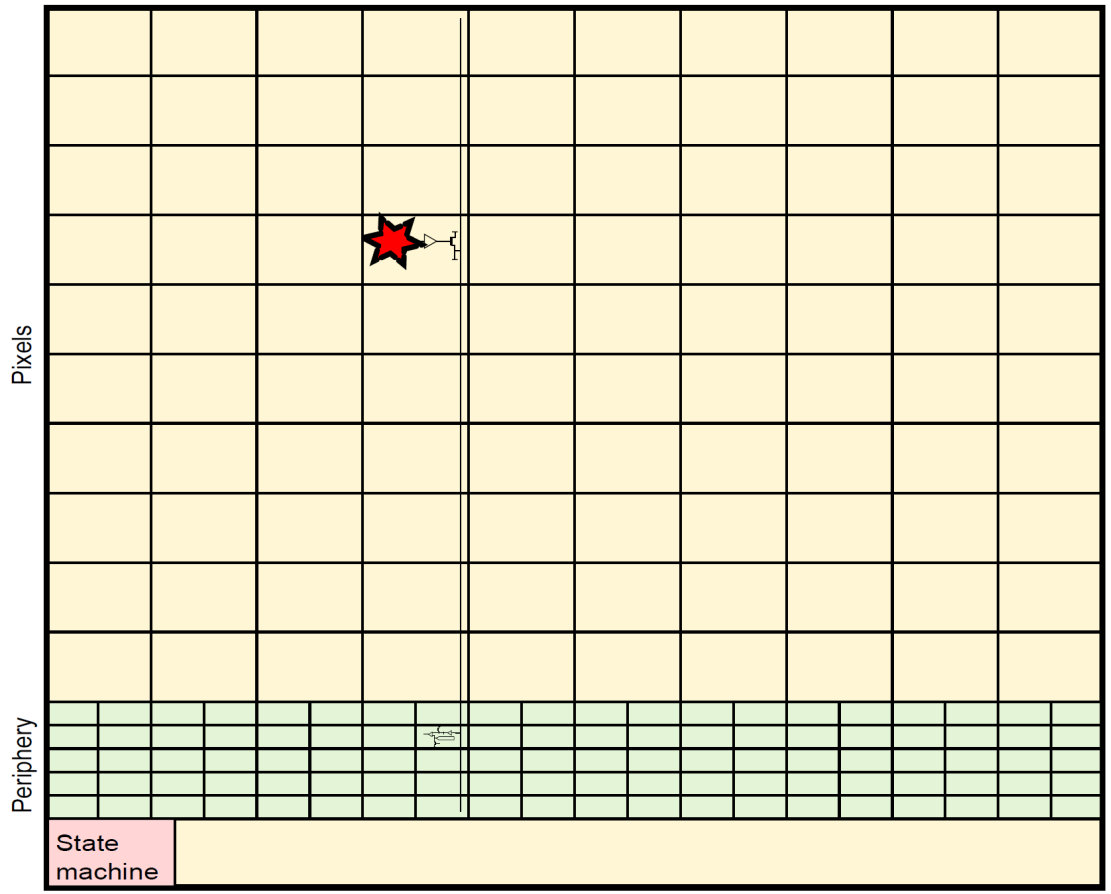


Pixel area

Pixel buffer area

Readout logic

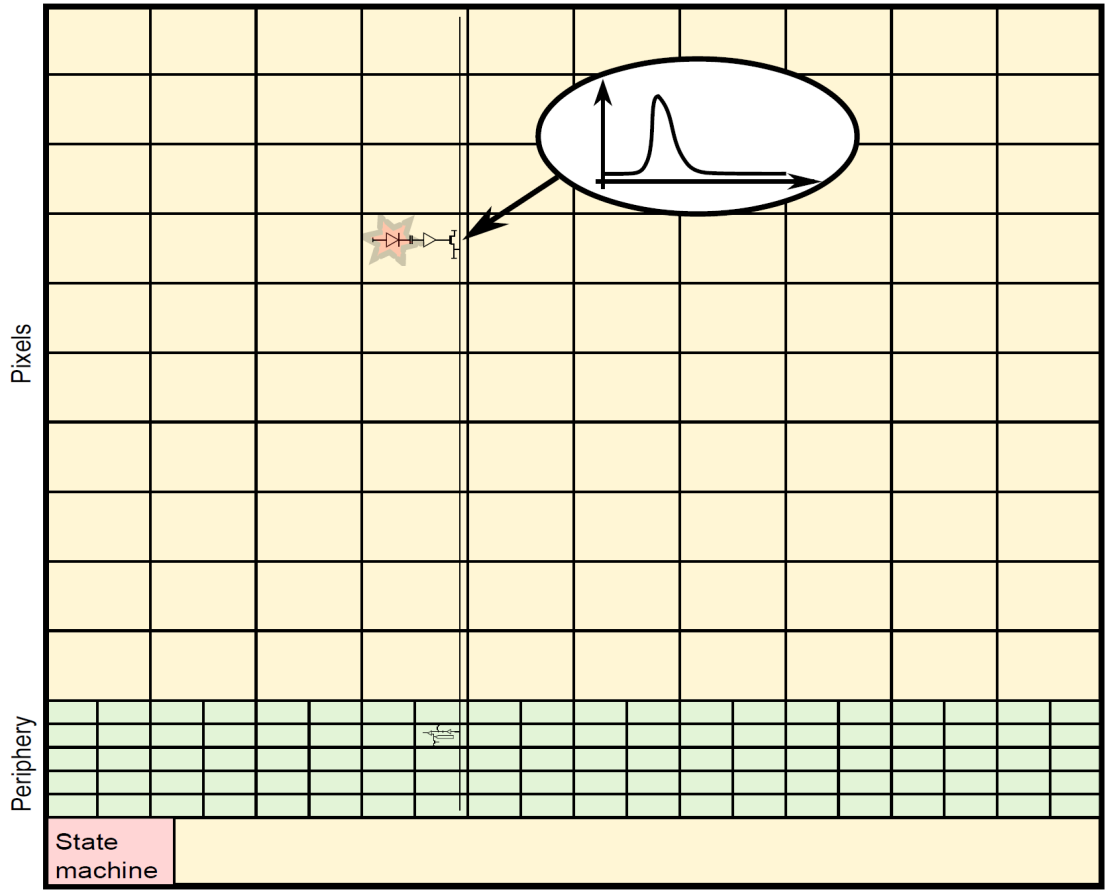
Summary of HV-MAPS operation



Event Sequence:

- **Signal**

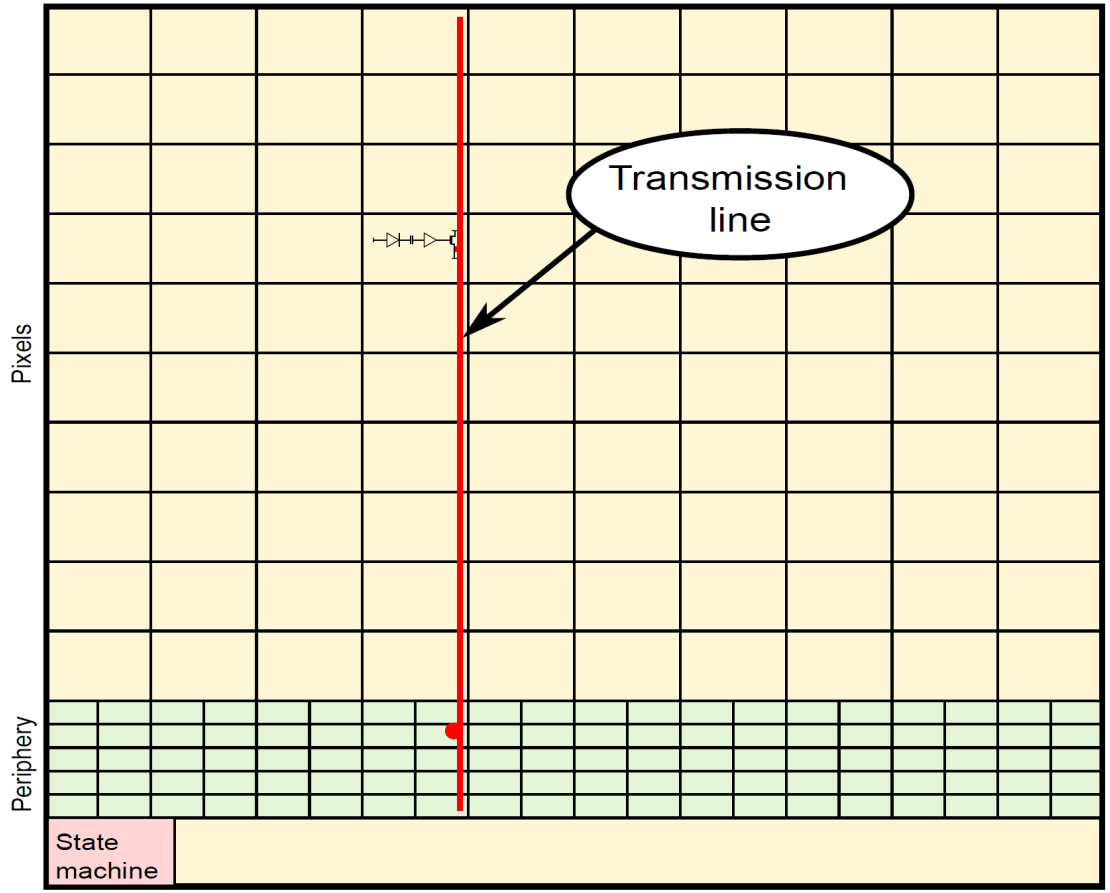
Summary of HV-MAPS operation



Event Sequence:

- **Signal**
- **Amplification**

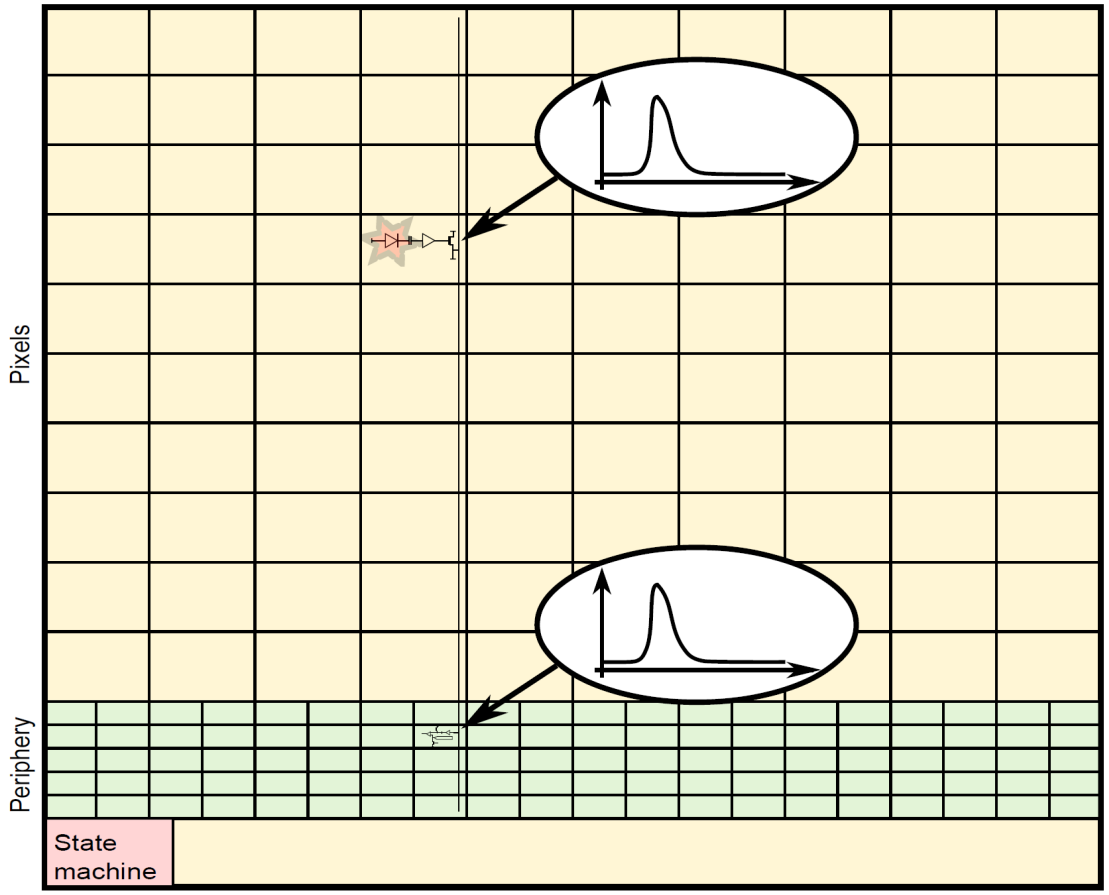
Summary of HV-MAPS operation



Event Sequence:

- **Signal**
- **Amplification**
- **Transmission to periphery**

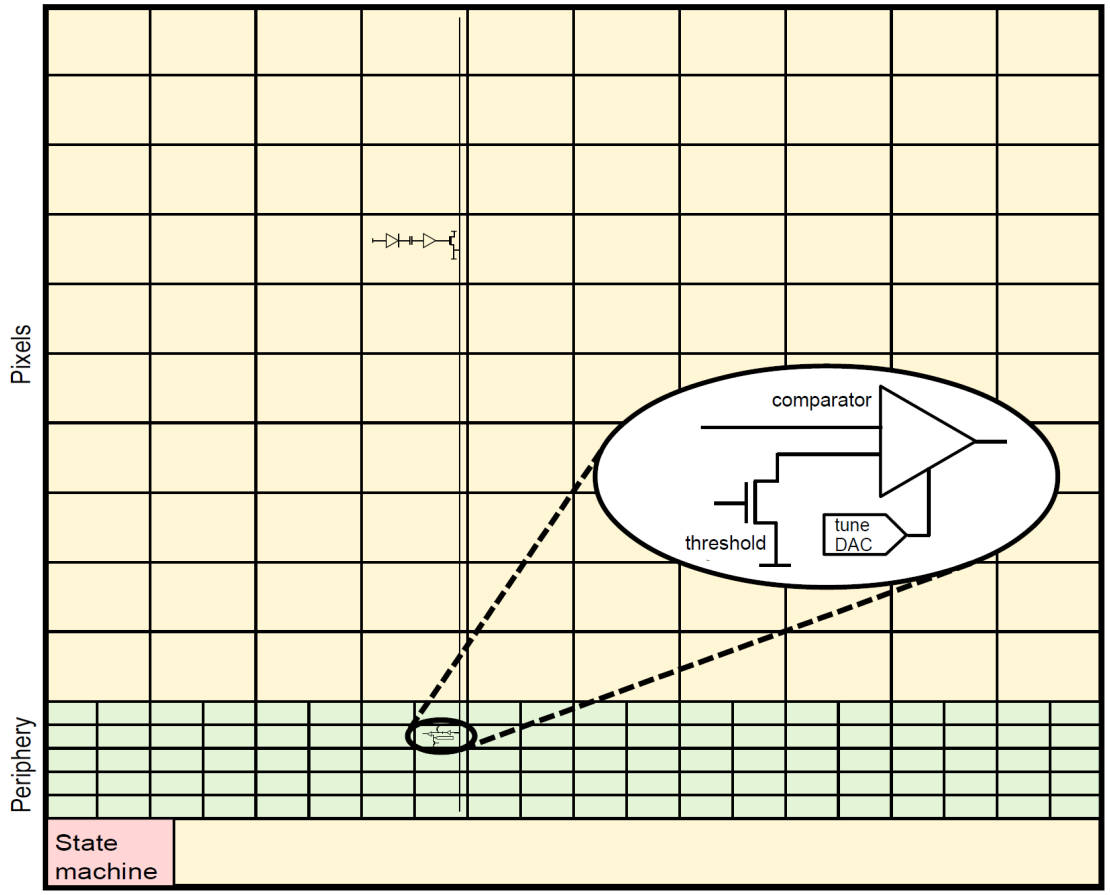
Summary of HV-MAPS operation



Event Sequence:

- Signal
- Amplification
- Transmission to periphery
- Storage in the buffer (pixel cleared for next event)

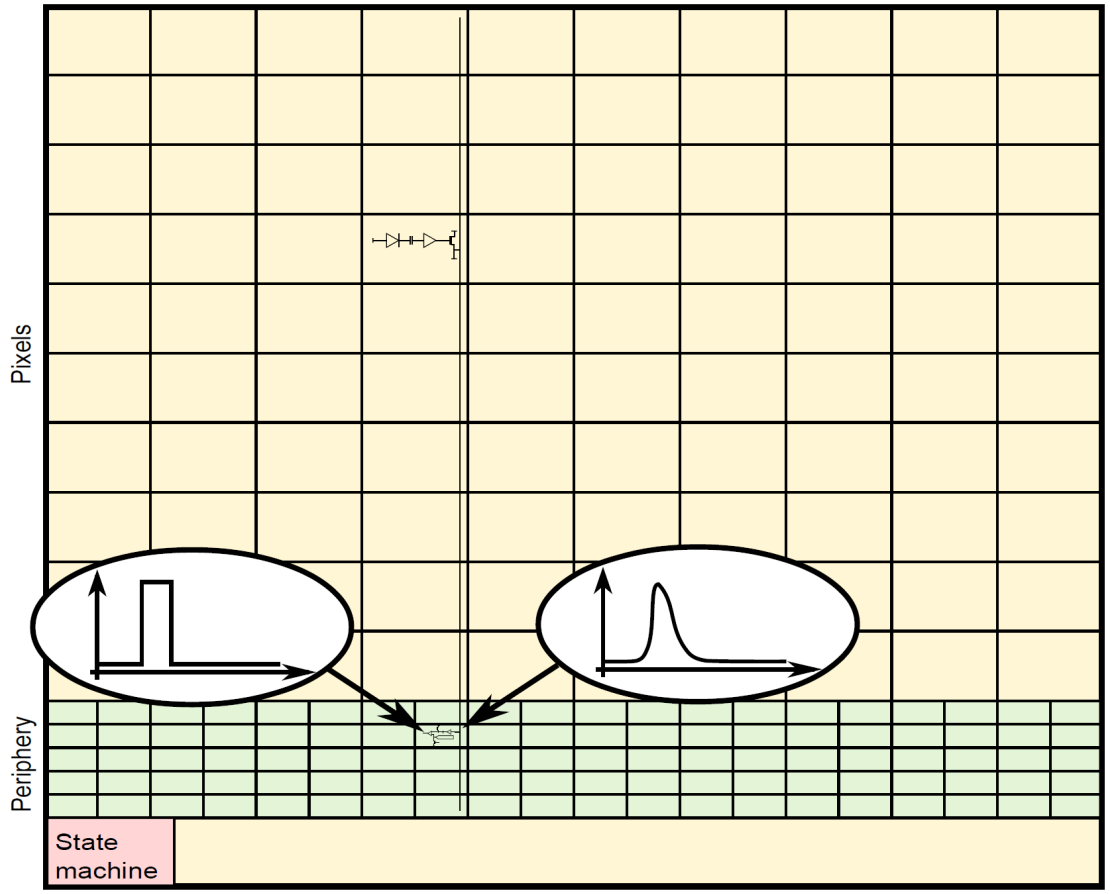
Summary of HV-MAPS operation



Event Sequence:

- **Signal**
- **Amplification**
- **Transmission to periphery**
- **Storage in the buffer (pixel cleared for next event)**
- **Digitization of the hit**

Summary of HV-MAPS operation



Event Sequence:

- Signal
- Amplification
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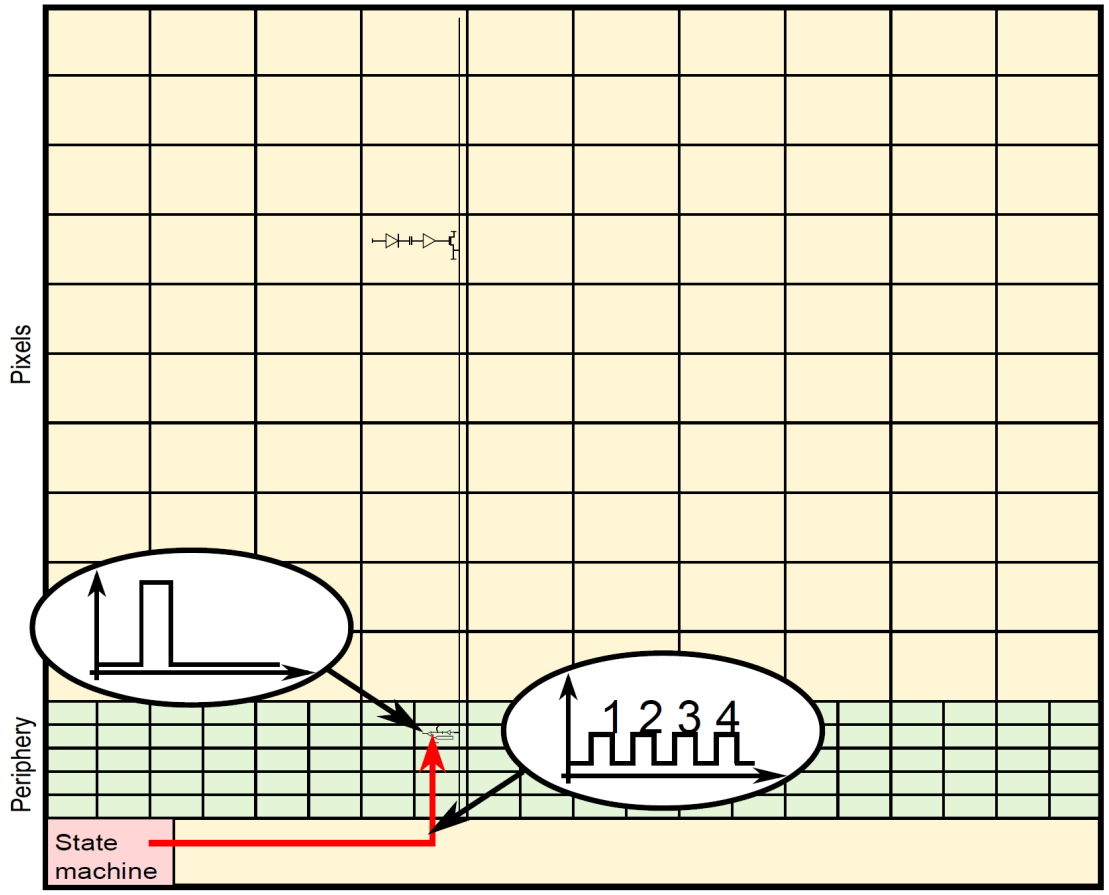
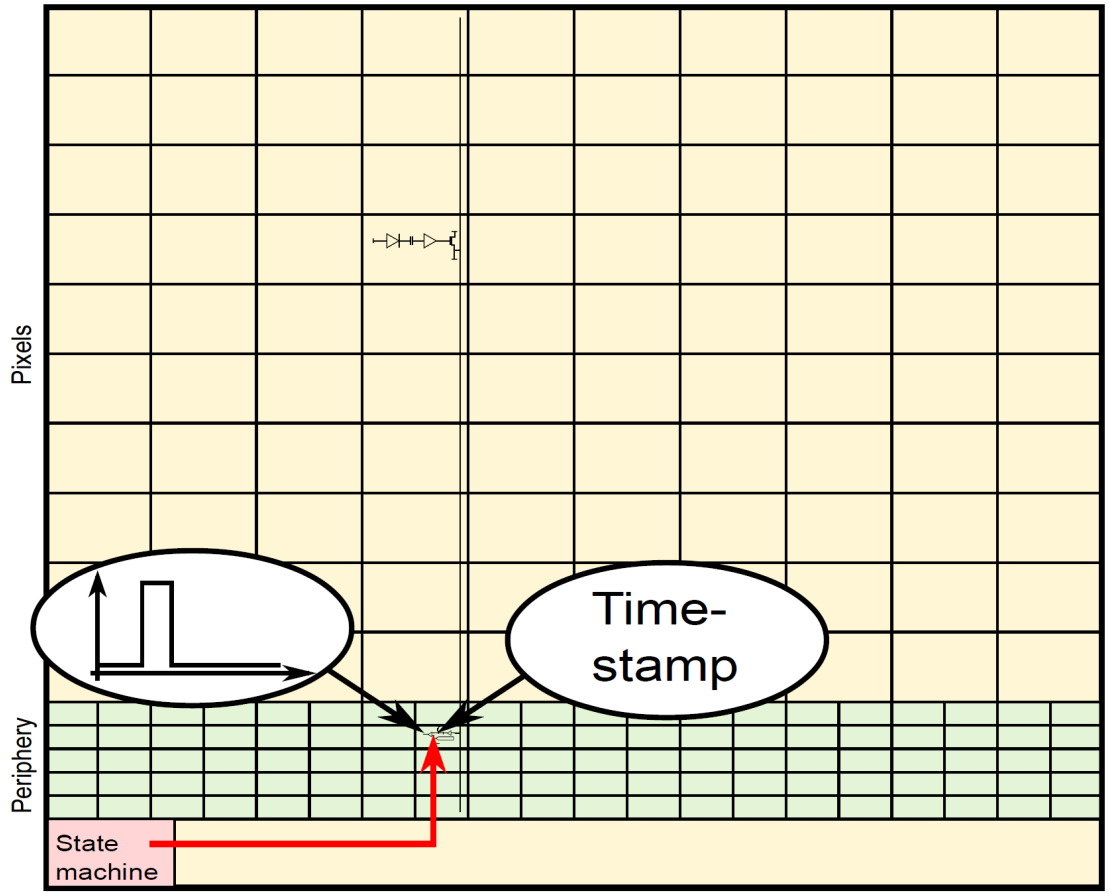
Summary of HV-MAPS operation



Event Sequence:

- Signal
- Amplification
- Transmission to periphery
- Storage in the buffer (pixel cleared for next event)
- Digitization of the hit
- Scalar generated from clk

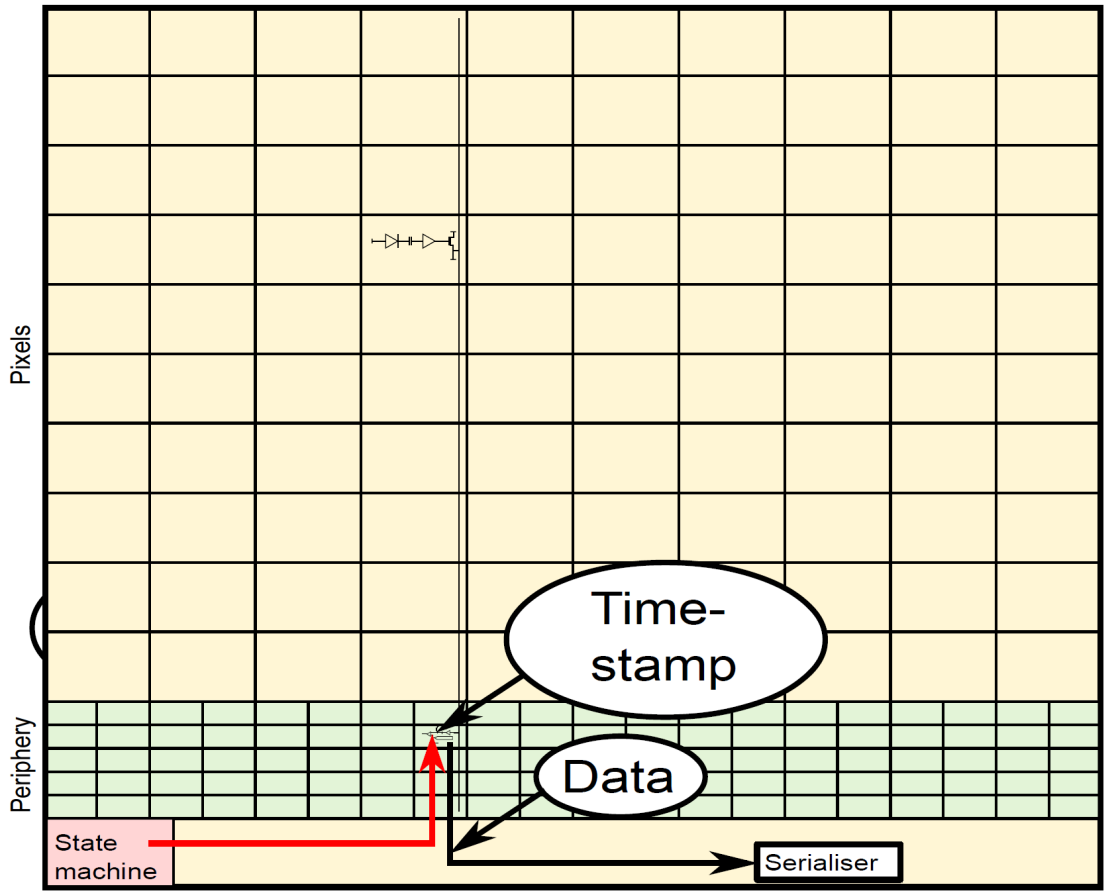
Summary of HV-MAPS operation



Event Sequence:

- Signal
- Amplification
- Transmission to periphery
- Storage in the buffer (pixel cleared for next event)
- Digitization of the hit
- Scalar generated from clk
- Timestamp generation

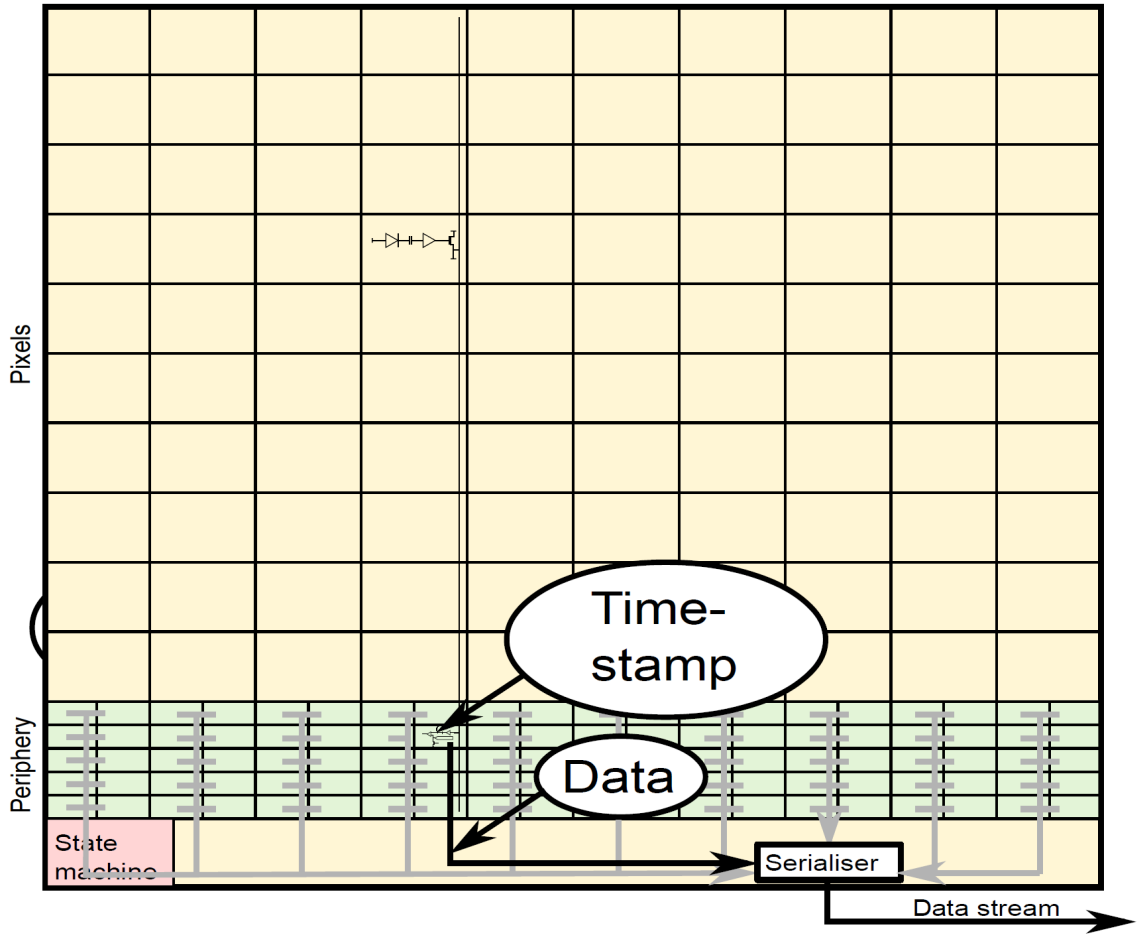
Summary of HV-MAPS operation



Event Sequence:

- Signal
- Amplification
- Transmission to periphery
- Storage in the buffer (pixel cleared for next event)
- Digitization of the hit
- Scalar generated from clk
- Timestamp generation
- Hit/pixel address and timestamp sent to serializer

Summary of HV-MAPS operation

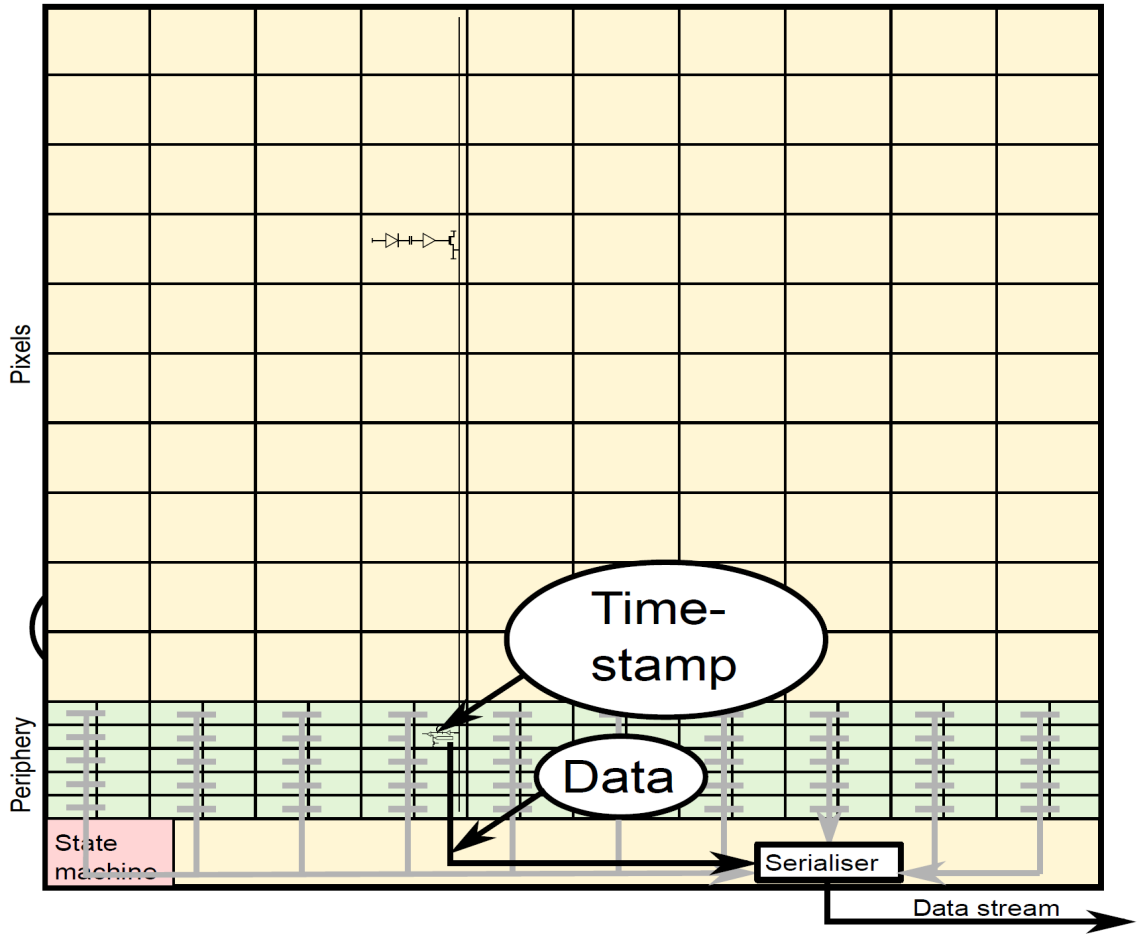


Event Sequence:

- **Signal**
- **Amplification**
- **Transmission to periphery**
- **Storage in the buffer (pixel cleared for next event)**
- **Digitization of the hit**
- **Scalar generated from clk**
- **Timestamp generation**
- **Hit/pixel address and timestamp sent to serializer**
- **Data sent to readout board**

Maximum readout rate is 33 MHz per link with a maximum of 3 links per chip.

Summary of HV-MAPS operation



Minor modifications to final chip:

- **Match the on-chip clk to the CERN readout chip frequency**
- **A simple AND with a GATE link before each pixel buffer to turn on/off the readout – timed to choice to reduce pixel occupancy**

These changes are relatively simple and underway.

Need to resubmit for one more engineering run

Then go to chip production – hopefully at the end of the year

Readout Setup

We need to design and prototype a readout board that incorporates 4 lpGBT chips and 1 VTRx+, plus bias and LV power supply distribution.

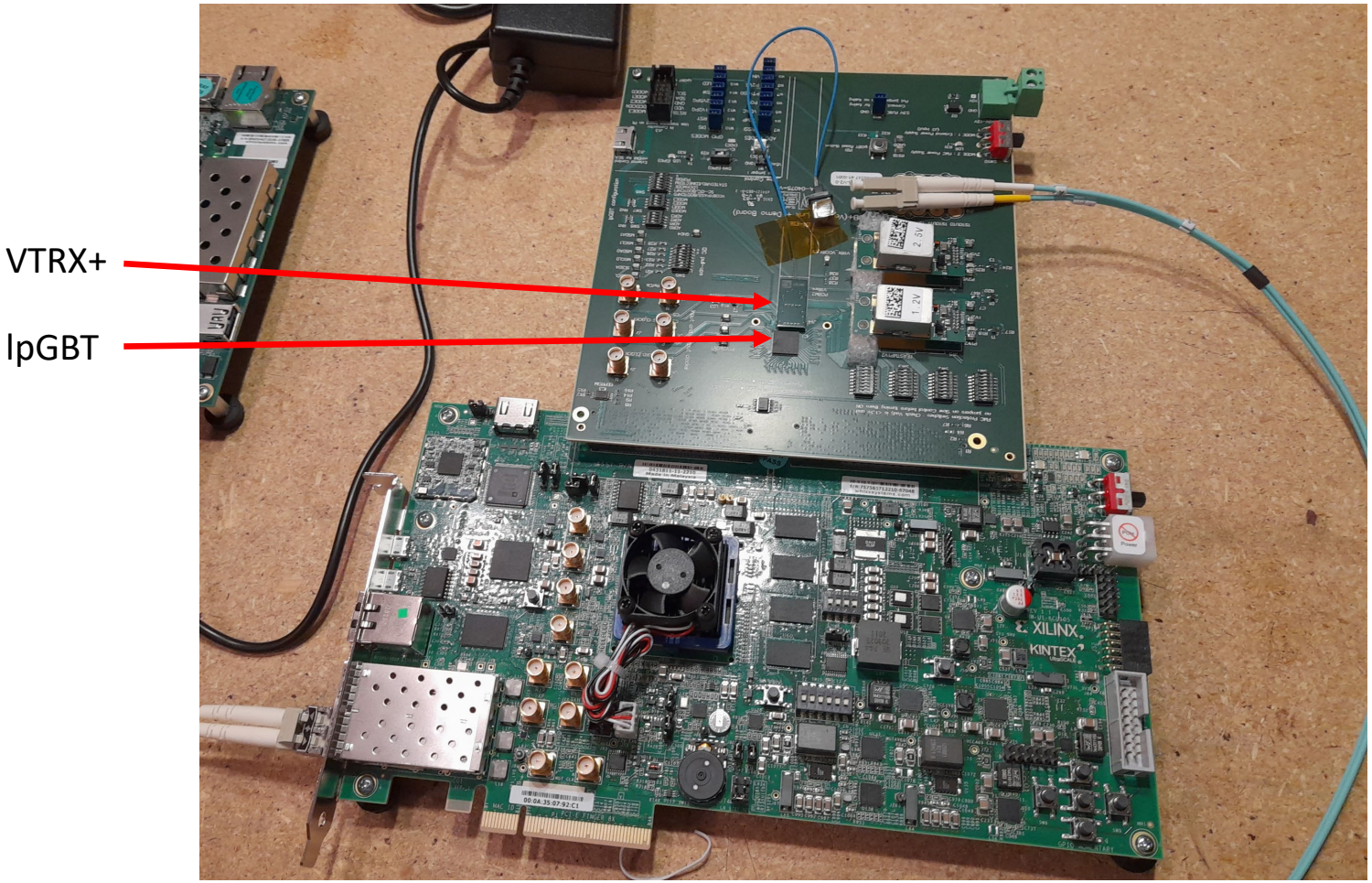
Starting point: The bord schematics/design is available to us from CERN.

We can remove quite a few of the test/diagnostic components and want to make the board smaller for the ring 5 detectors, while incorporating 4 lpGBTs rather than 1.

Development is ongoing:

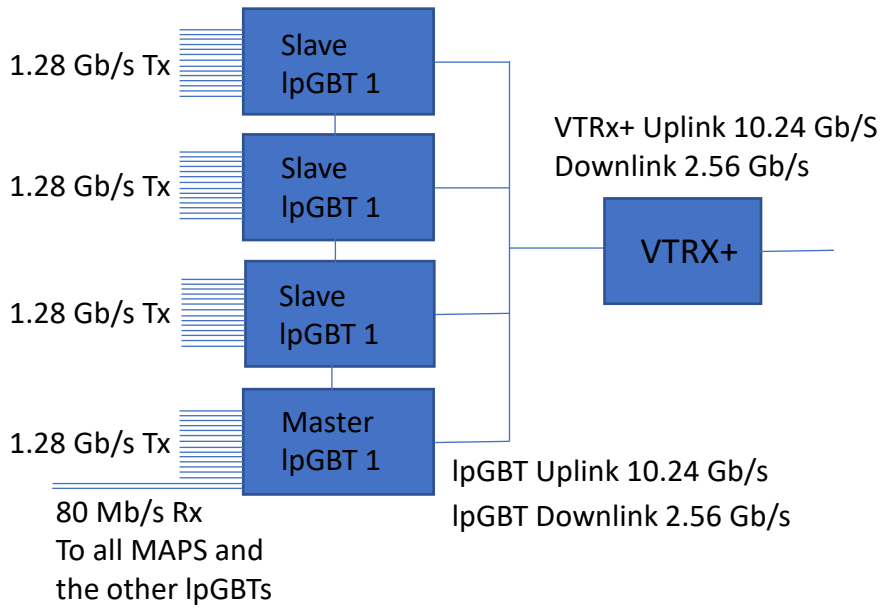
We have access to an engineer at Carleton Univ. through the Canadian SAP Major Resources Support network

To be mostly completed by end of June



Readout Setup:

- We want 3 lpGBTs in slave mode and 1 lpGBT as master
- Slow-Control the lpGBTs via the of the down/uplink data stream from the back-end FPGA . This field allows to read and write the internal registers if the chip operates as a Transceiver (master).
- The VTRX+ has 4 uplinks (10.24 Gb/s) and one downlink (2.56 Gb/s) so we can read out
- Need to determine if we need the FEASTMP DC/DC converters or can run via remote power control
- We can use the Samtec ASP-134486-01 FMC connector (female)
- Maximum board width 100 mm
- Maximum board length 200 mm
- Mounting holes can be relocated within the lower 50 mm of the board.



Readout Setup:

Conceptual schematic of the readout and control setup.

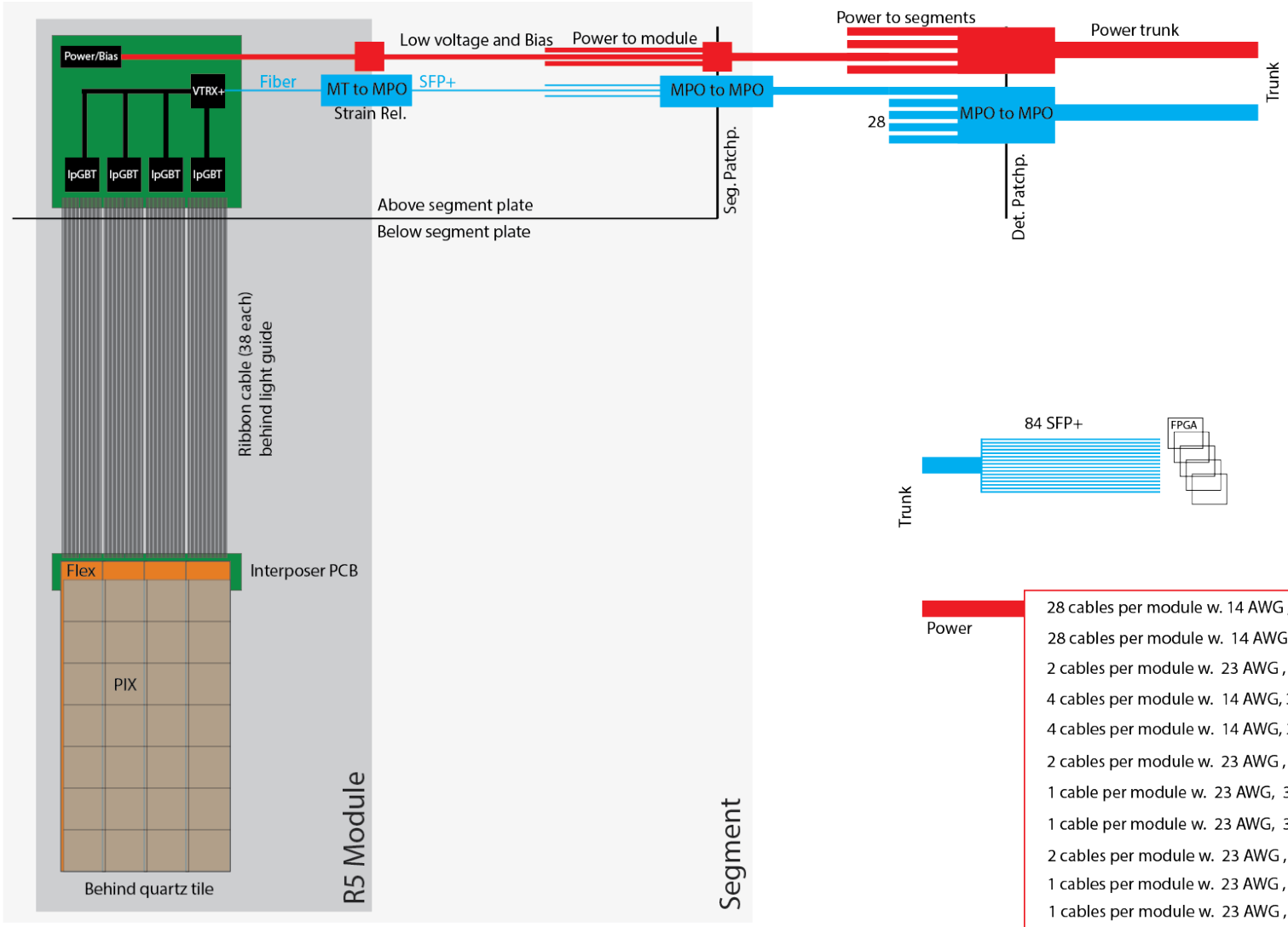
With 1.28Gb/s (TX) und 80 Mb/s (RX) we can read out 7 MAPS with one lpGBT.

Use 3 lpGBT as simplex transmitter and 1 lpGBT as transceiver (same mode as used by CMS).

Using this configuration we can use one VTRx+ to read out 28 MAPS

TX = Detector → Counting Room,

RX = Counting Room → Detector



Readout Setup:

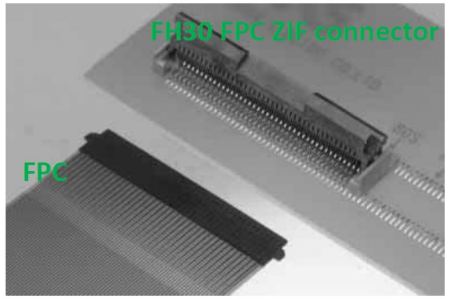
Flexprint design (Jie Pan)

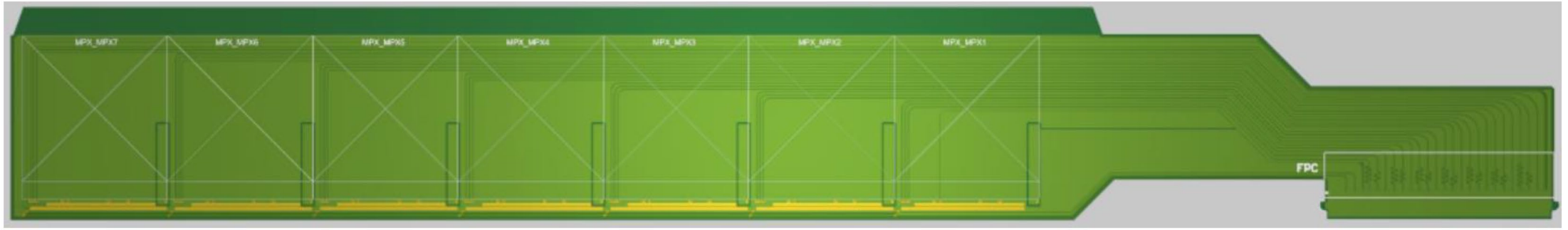
- Design Considerations:
- Maintain insolation and distance for HV bias
- Impedance control for differential pairs
- Minimize cross-talks
- Trace delay tuning for high-speed signal synchronization
- Edge overlap design to minimize gaps between strips
- Arrange high density connectors sideway to ease the assembly and installation
- Maximize widths of power and ground traces to allow large current flow at minimized low
- voltage drops

For each Ring 5 Quartz tile: TAB-bond 7 chips to a flex-print, have 4 such strips per detector

For each Ring 5 Quartz tile: TAB-bond 7 chips to a flex-print, have 4 such strips per detector

Simple FPC insertion
Flip-lock

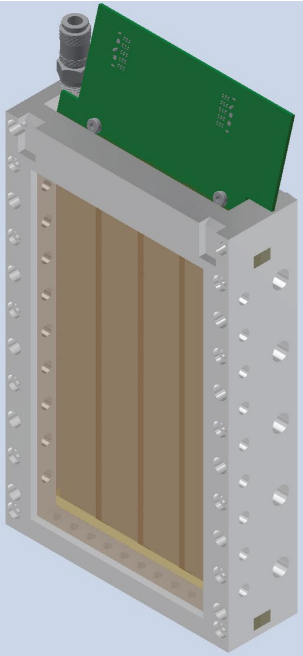


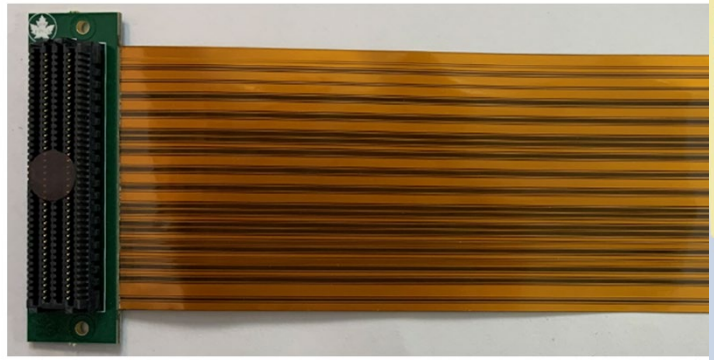


Design is done, preparing for making prototypes

Mounting:

Ring 5 Quartz tile HVMAPS in the MD array:



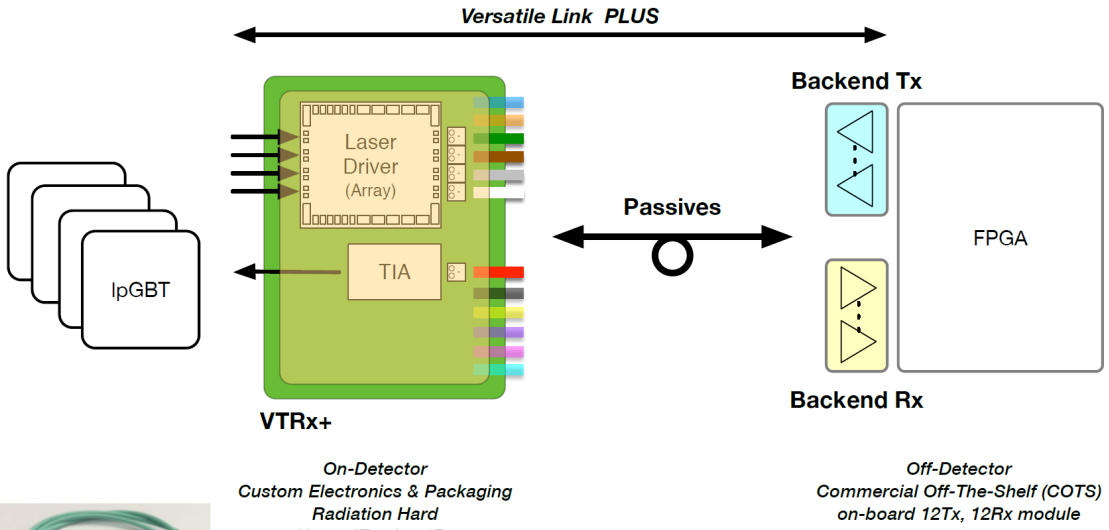


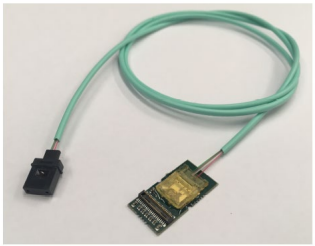
More updated mounting geometry in Kristofer's talk

Back-end DAQ:

- Need an array of commercial FPGA boards like the Xilinx kcu105
- Or something like the Arista 48/96 LS fiber switch

From VTRX+ CERN Manual





Hardware

Description		Price	Qty	Ext. Price
DCS-7130-48LS-F	**Arista 7130 Series 48L with UltraScale VU7P-2 FPGA, front-to-rear air, 2xAC v2**	$31,027.07	1	$31,027.07
SVC-7130-48LS-1M-NB	**1-Month A-Care Software & NBD Hardware Replacement/Same Day Ship for 7130-48LS**	$294.55	60	$17,673.00
DCS-7130-96LS-F	**Arista 7130 Series 96L with UltraScale VU7P-2 FPGA, front-to-rear air, 2xAC v2**	$51,041.78	1	$51,041.78
SVC-7130-96LS-1M-NB	**1-Month A-Care Software & NBD Hardware Replacement/Same Day Ship for 7130-96LS**	$483.06	60	$28,983.60
SFP-10G-SR-P	**Arista 10GBASE-SR SFP+ (Short Reach)**	$74.80	48	$3,590.40
TARIFF FEE	**Logistics Fee**	$8,258.66	1	$8,258.66
FREIGHT.	**Shipping & Handling**	**$150.00**	**1**	**$150.00**
			Subtotal:	**$140,724.51**

Quote Summary	Amount
Hardware	$140,724.51
Subtotal:	**$140,724.51**
Estimated GST:	**$7,036.22**
Estimated PST:	**$9,850.71**
Total:	**$157,611.44**

Main detector low voltage cables and power supplies

2. HVMAPS

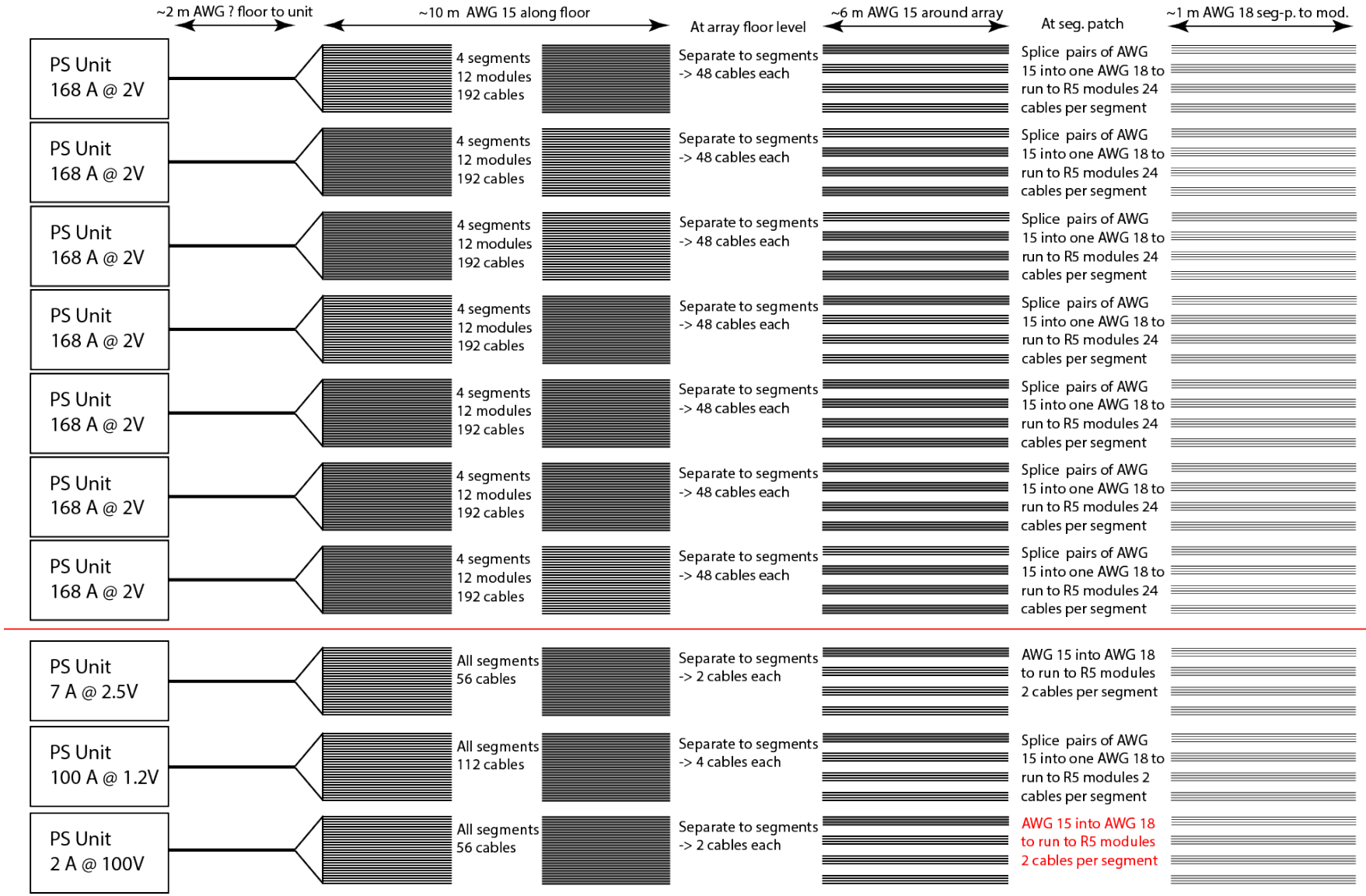
- 84 modules with 28 chips per module. Need three different LV connections for each module ($2V, 1.2V, 2.5V$) and one "HV" connection ($\lesssim 100\ V$) for bias
- LV powers the chip itself and the readout electronics

Per Module:

- Chip supply voltage: $V_{chip} = 2V\ @\ 0.5A\ \times\ 28$ (parallel)
- Readout lpGBT: $V_{lpBGT} = 1.2V\ @\ 0.27A \times 4$
- Readout VTRX+: $V_{VTRX} =\ 1.2V\ @\ 0.045A + 2.5V\ @\ 0.080A$
- Bias: $V_{bias} =\ 100V\ @\ 0.02A$
- Largest power: $P_{chips} \simeq 34\ W$ (includes ~20% safety factor)
- Total power: $P_{tot} \simeq 38\ W$ (includes ~20% safety factor)

Cables:

- Voltage drops:
  - Flexprint to R5 readout: $\Delta V{\sim}0.15V\ @\ 3.5\ A$
  - R5 readout to segment patch panel: $\Delta V{\sim}0.16V\ @\ 3.5\ A$ AWG 18 (VDD + GND = 24 cables/segment)
  - Segment patch panel to GEM hut: $\Delta V{\sim}0.56V\ @\ 1.75\ A$ AWG 15 (Split VDD and GND into two AWG 15 = 48 cables)
  - GEM hut floor to PS unit: $\Delta V{\sim}0.12V\ @\ ?\ A$ AWG ? (Depends on PS unit we choose)
  - Total: $\Delta V \leq 1V$ (Depending on PS unit we chose)


~2 m AWG ? floor to unit
~10 m AWG 15 along floor
At array floor level
~6 m AWG 15 around array
At seg. patch
~1 m AWG 18 seg-p. to mod.
PS Unit 168 A @ 2V
4 segments 12 modules 192 cables
Separate to segments -> 48 cables each
Splice pairs of AWG 15 into one AWG 18 to run to R5 modules 24 cables per segment
Chips
PS Unit 7 A @ 2.5V
All segments 56 cables
Separate to segments -> 2 cables each
AWG 15 into AWG 18 to run to R5 modules 2 cables per segment
PS Unit 100 A @ 1.2V
All segments 112 cables
Separate to segments -> 4 cables each
Splice pairs of AWG 15 into one AWG 18 to run to R5 modules 2 cables per segment
PS Unit 2 A @ 100V
All segments 56 cables
Separate to segments -> 2 cables each
AWG 15 into AWG 18 to run to R5 modules 2 cables per segment
Readout

Main detector low voltage cables and power supplies

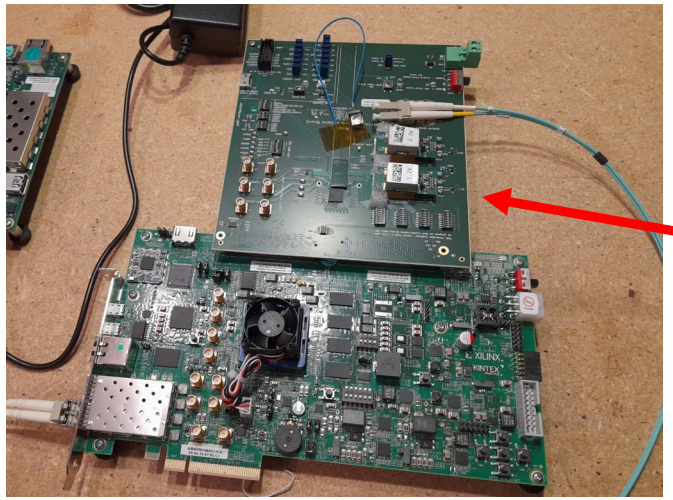
2. HVMAPS

PSU Series

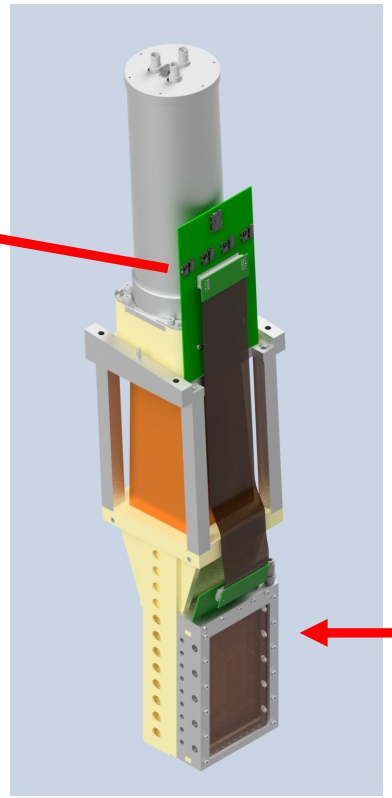
- Single channel high current

SPECIFICATIONS	
MODEL	PSU 6-200
OUTPUT RATINGS	
Rated Output Voltage (*1)	6V
Rated Output Current (*2)	200A
Rated Output Power	1200W
RIPPLE AND NOISE(*5)	
CVp-p(10 ~ 20MHz) p-p (*6)	60mV
CVrms(5Hz ~ 1MHz) r.m.s. (*7)	8mV
CCrms(5Hz ~ 1MHz) r.m.s.(*12)	400mA
LOAD REGULATION	
Voltage(*4)	2.6mV
Current(*11)	45mA
LINE REGULATION	
Voltage(*3)	2.6mV
Current(*3)	22mA

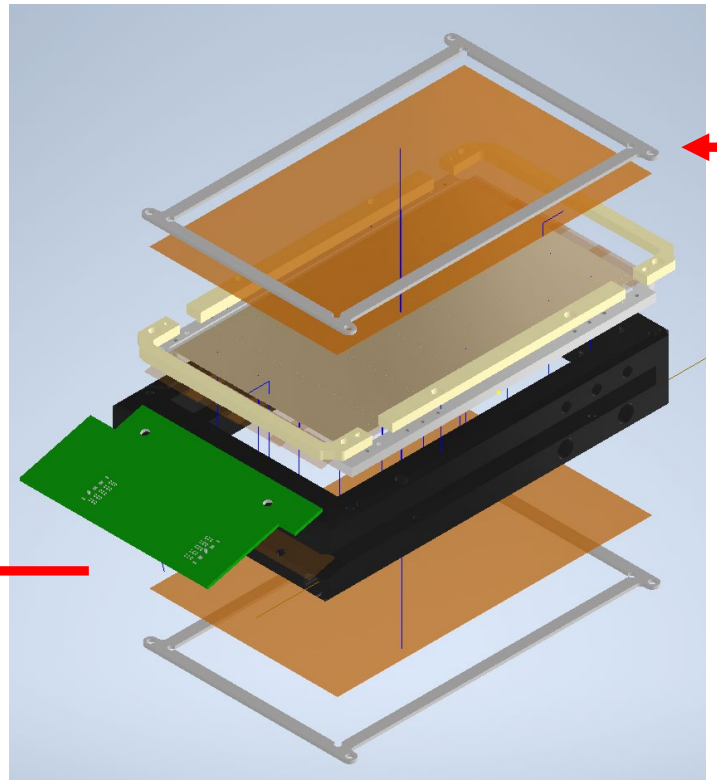
Backups

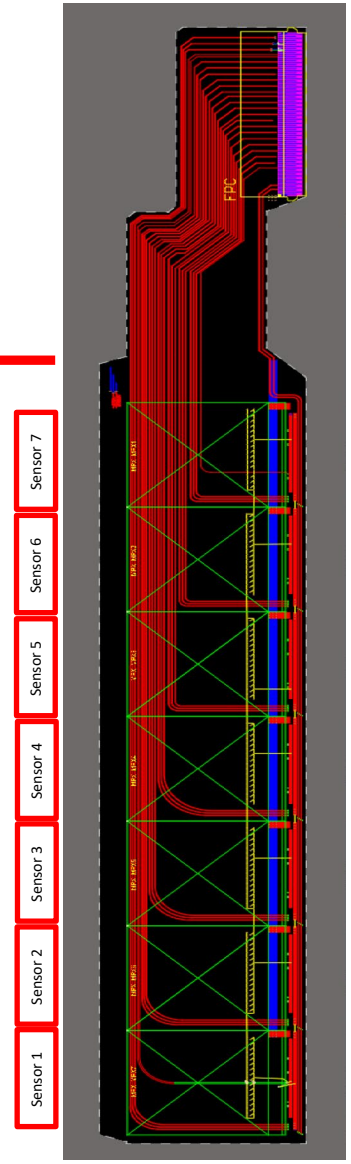


CERN Developed readout test board. With FPGA backend.



Work by Kristofer Isaak UManitoba

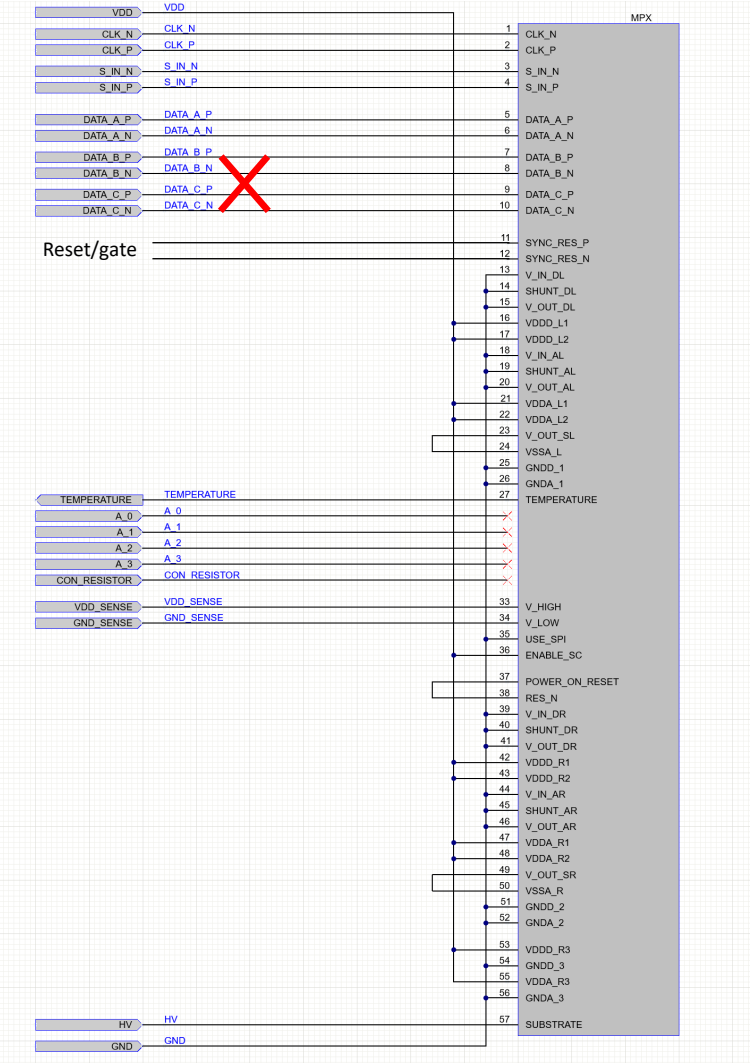




Readout Setup:

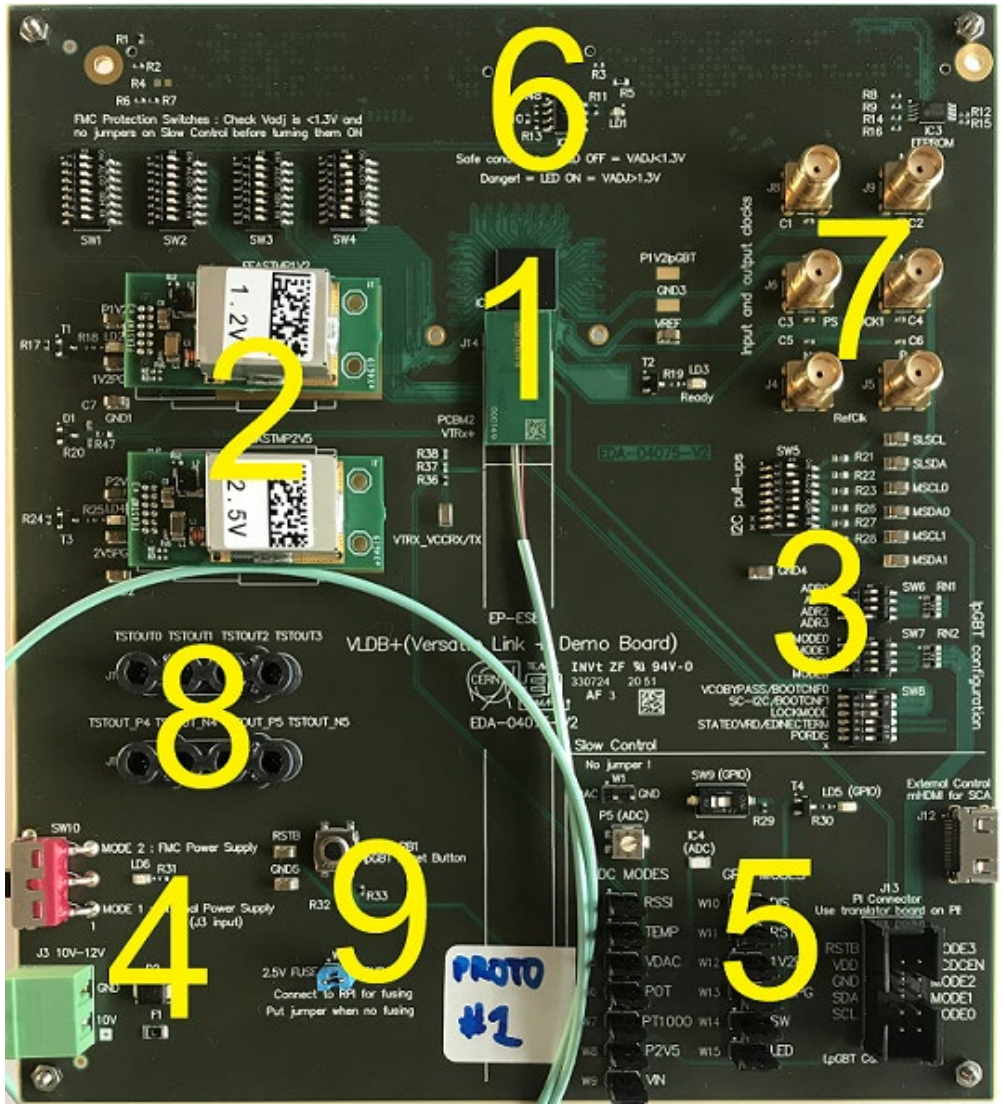
Chip-to-flexprint connections:

- Single LVDS pair readout per chip at ~180 Mbps
- 7 chips ~ 1.28 Gbps
- 14 lines per chip through flexprint and ribbon
- Clk_P/N from lpGBT
- S_In_P/N chip addressing through lpGBT slow control
- SYNC_RES_P/N chip gating (or similar) also through lpGBT
- Rest of the lines are voltage distribution

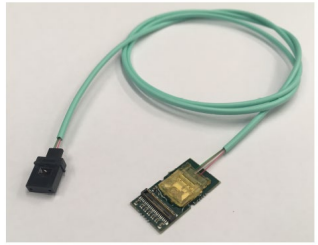


VLDB:

- Item 1: Core parts needed – 4 lpGBT, 1 VTRX+
- Item 2: FEASTMP may not be needed. Use remote power from PS unit (see slide 6) – need to implement a sense wire – maybe can use them though
- Item 3: Not needed - mode selection should take place via the downlink interface
- Item 4: Needs to be re-designed to supply power to the lpGBTs , the VTRX+, and to the HCMAPS chips
- Item 5: Not needed – startup configuration and operation mode need to be “hard wired” by pulling control pins high/low with resistors
- Item 6: Not needed
- Item 7: Not needed – reference clock should come through downlink, but the lower two connectors could be kept for benchtop testing/prototyping
- Item 8: Could be kept for prototype testing
- Item 9: Not needed but might be useful for testing

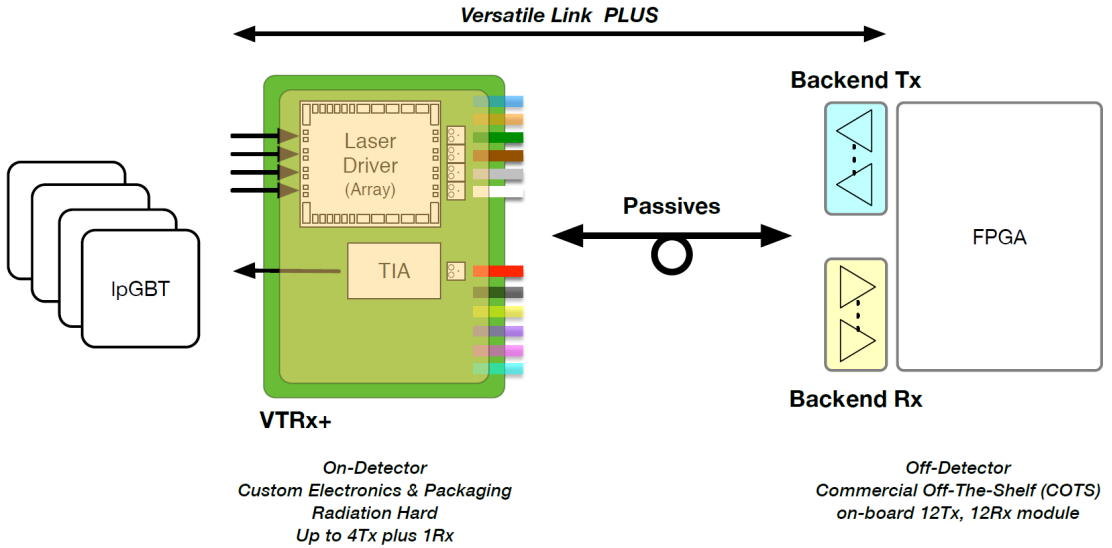


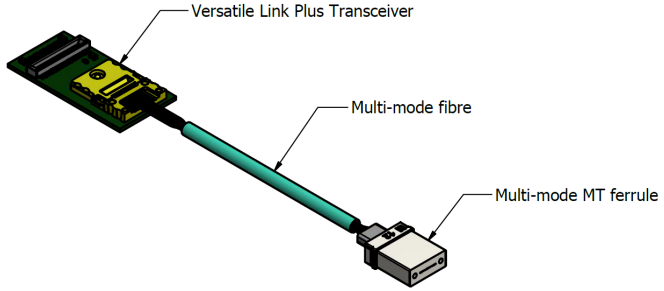
VTRX+ Info:

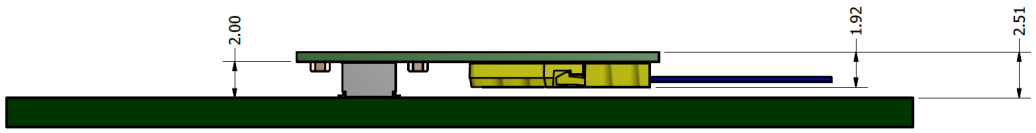


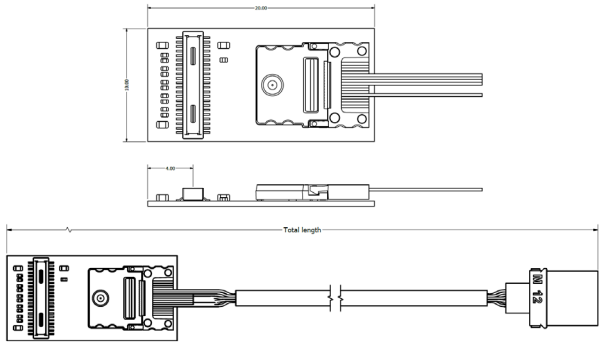
- Fiber optic transceiver
- 4 upstream channels (sum = 10.24 Gb/s)
- 1 downstream channel (2.56 Gb/s)
- 20 cm pigtail with female MT terminator
- Needs to have MT-MPO (male) adapter or other to connect to standard fiber

From VTRX+ CERN Manual



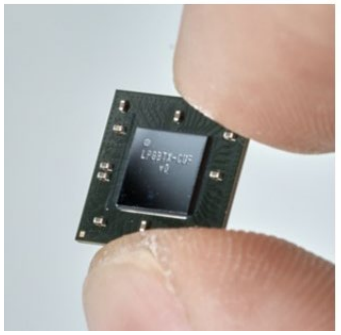




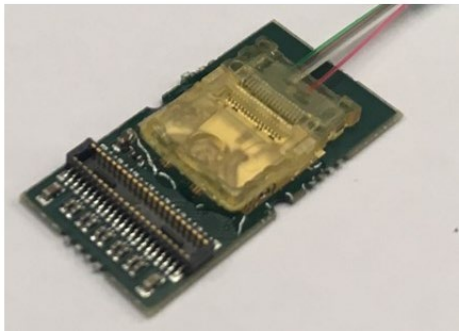


CERN Chips Details

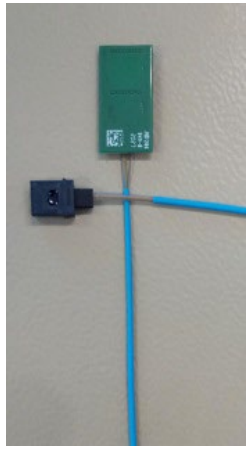
lpGBT



VTRx



New

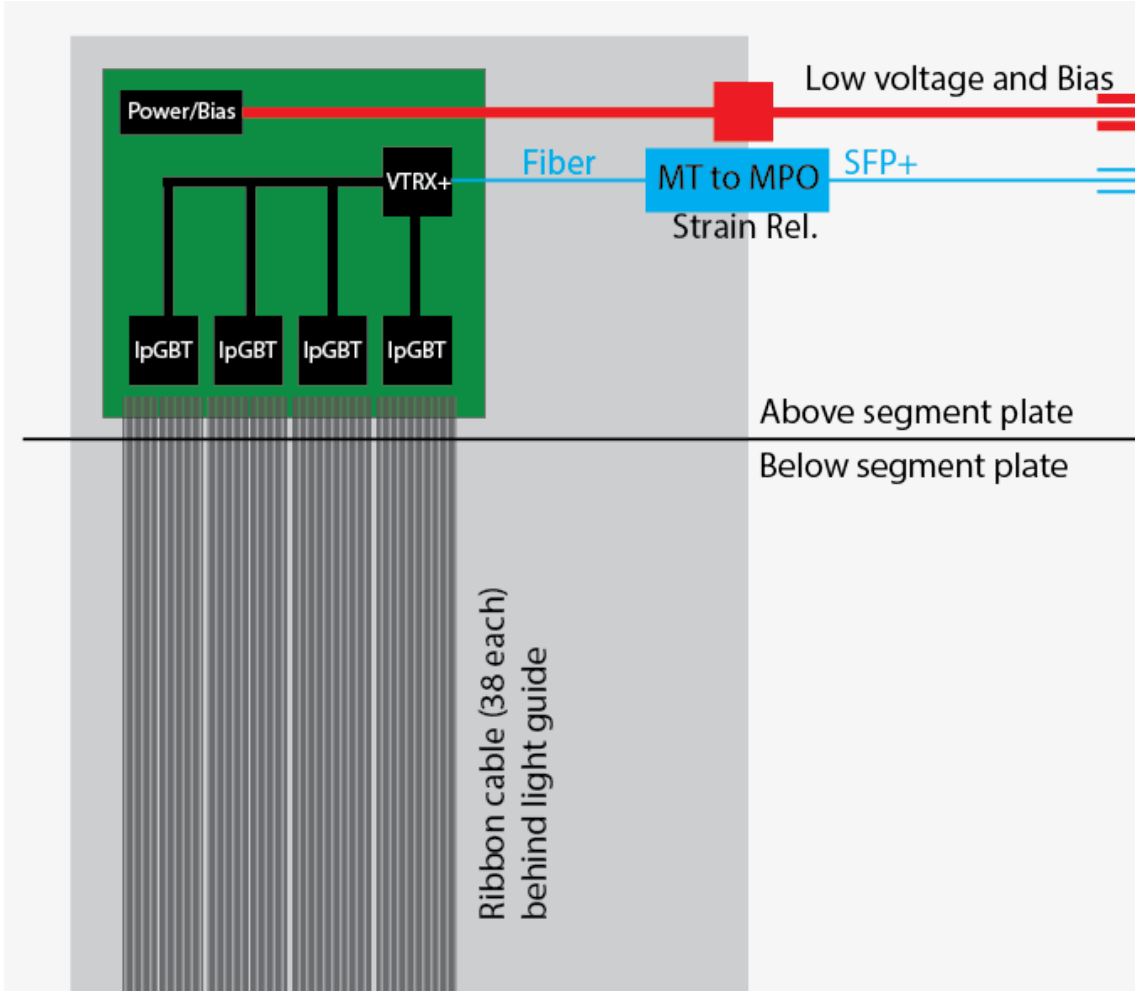


New HVMAPS chip production to start in 2023:

- Implement gated readout from chip
- Adjust design to match the lpGBT protocol
- Can use one lpGBT for 7 HVMAPS
- Can use one VTRx for 4 lpGBT chips
- Readout 28 HVMAPS with this combination
- Need 84 fiber connections (VTRx)
- Need 336 of the lpGBT chips
- Readout (TX) at 1.28 Gb/s
- RX at 160 Mb/s

Status:

- CERN shipped all of the lpGBT chips to Manitoba
- VTRX+ chips are coming in the next few months
- We have one of the CERN prototype readout boards. The VTRx+ can be used for prototype development
- Design of the MAPS module, flexprint, cooling, interposer is progressing well
- Commercial Xilinx FPGA backend solution is being identified and priced out
- Power supply and bias system (cabling and control) is currently based on direct remote control, but possible DC/DC conversion closer to the readout board is being considered.



Summary of HV-MAPS operation

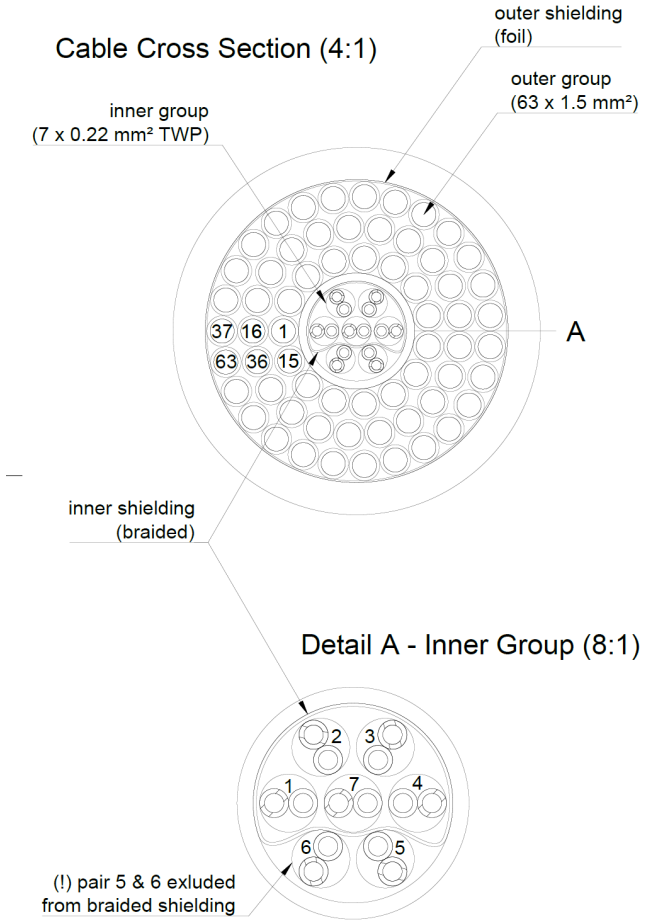
- Chip connections:

    1. There will be 4 differential outputs (8 lines) per chip that are connected to the lpGBT:
        1. Clock (Clk_n/p)
        2. Data-out (DOut_n/p)
        3. Gate_n/p
        4. Addressing (Sin_n/p)

    2. There could be one more digital temperature signal from each chip to the lpGBT input (TBD)
    3. All signals except the temperature diode are LVDS
    4. Target TX speed is 1.28 Gbps (~180 Mbps per chip to lpGBT)
    5. Target RX speed is 80 Mbps (from lpGBT to chip)

Power and Bias

- Remote LV control cable design for the HVMAPS tracking detector
- We would need ~2 of these per segment
- Shorter cable is definitely better …
- We would need three fiber connections per segment

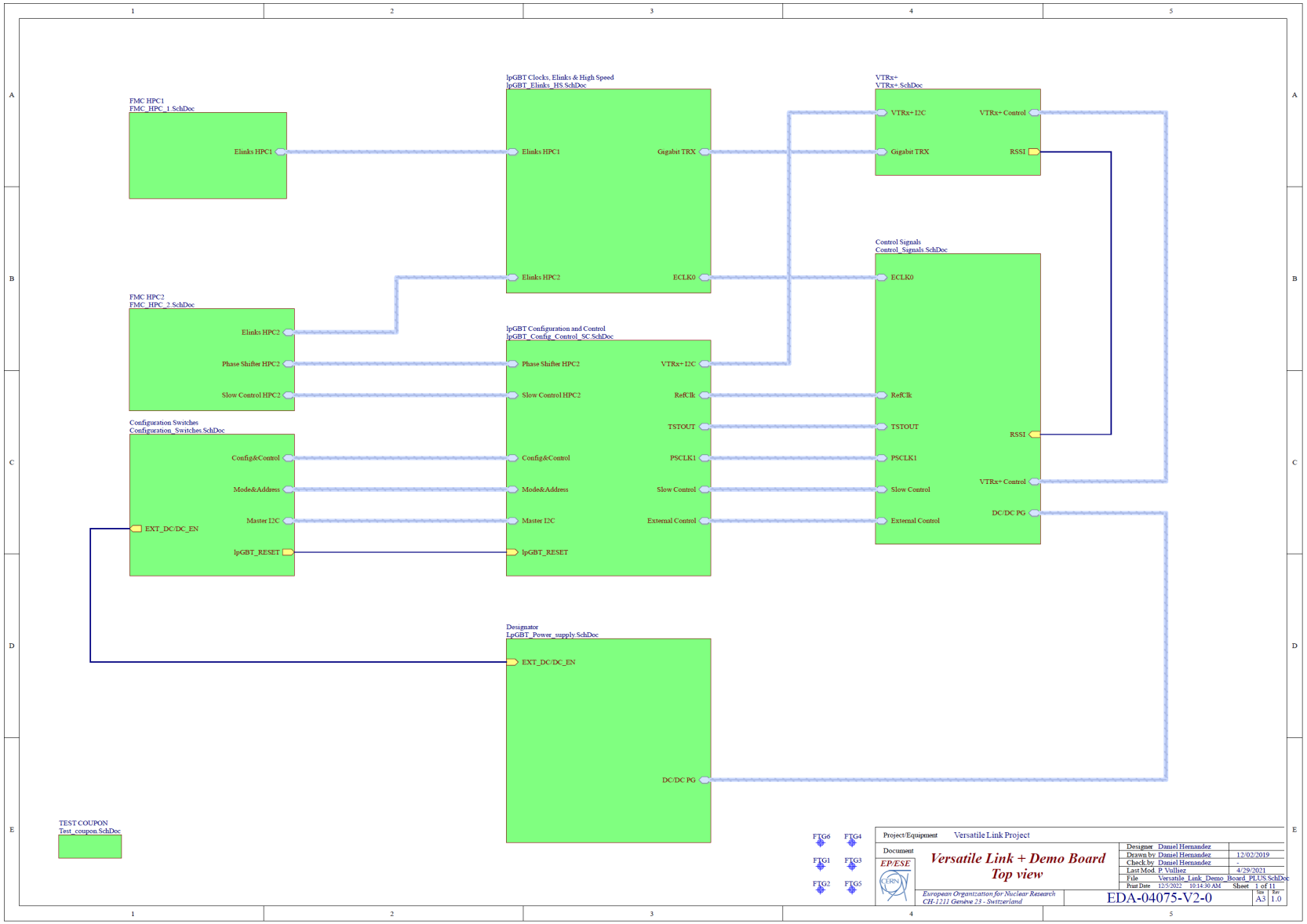


Outer Group			
Conductor No.	**Count x Colour**	**Construction**	**Electrical**
1, 3, 5, 7, 9, 11, 13, 19, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 45, 47, 49, 51, 53, 55, 57, 59, 61	29 x RD	1.5 mm² (65 x Ø0.16)	27 A @ 2.0 V
15, 63	2 x WH	1.5 mm² (65 x Ø0.16)	2.25 A @ 1.2 V
17	1 x BL	1.5 mm² (65 x Ø0.16)	0.4 A @ 2.5 V
2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 44, 46, 48, 50, 52, 54, 56, 58, 60, 62	31 x BK	1.5 mm² (65 x Ø0.16)	29.65 A @ 0 V (RTN)

Inner Group			
Pair No.	**Colour**	**Construction**	**Electrical**
1	GN-WH	2 x 0.22 mm² (7 x Ø0.203)	RSEN_2V0_P (2 V nom.)
	GN		RSEN_2V0_N (RTN)
2	YE-WH	2 x 0.22 mm² (7 x Ø0.203)	RSEN_1V2_P (1.2 V nom.)
	YE		RSEN_1V2_N (RTN)
3	RD-WH	2 x 0.22 mm² (7 x Ø0.203)	RSEN_2V5_P (2.5 V nom.)
	RD		RSEN_2V5_N (RTN)
4	BK-WH	2 x 0.22 mm² (7 x Ø0.203)	RSEN_HV_P (100 V nom.)
	BK		RSEN_HV_N (RTN)
5	GY-WH	2 x 0.22 mm² (7 x Ø0.203)	10 mA @ 100 V
	GY		10 mA @ 0V (RTN)
6	PK-WH	2 x 0.22 mm² (7 x Ø0.203)	10 mA @ 100 V
	PK		10 mA @ 0V (RTN)
7	BN-WH	2 x 0.22 mm² (7 x Ø0.203)	TBD
	BN		TBD

Appendix:

CERN Prototype Board Schematics



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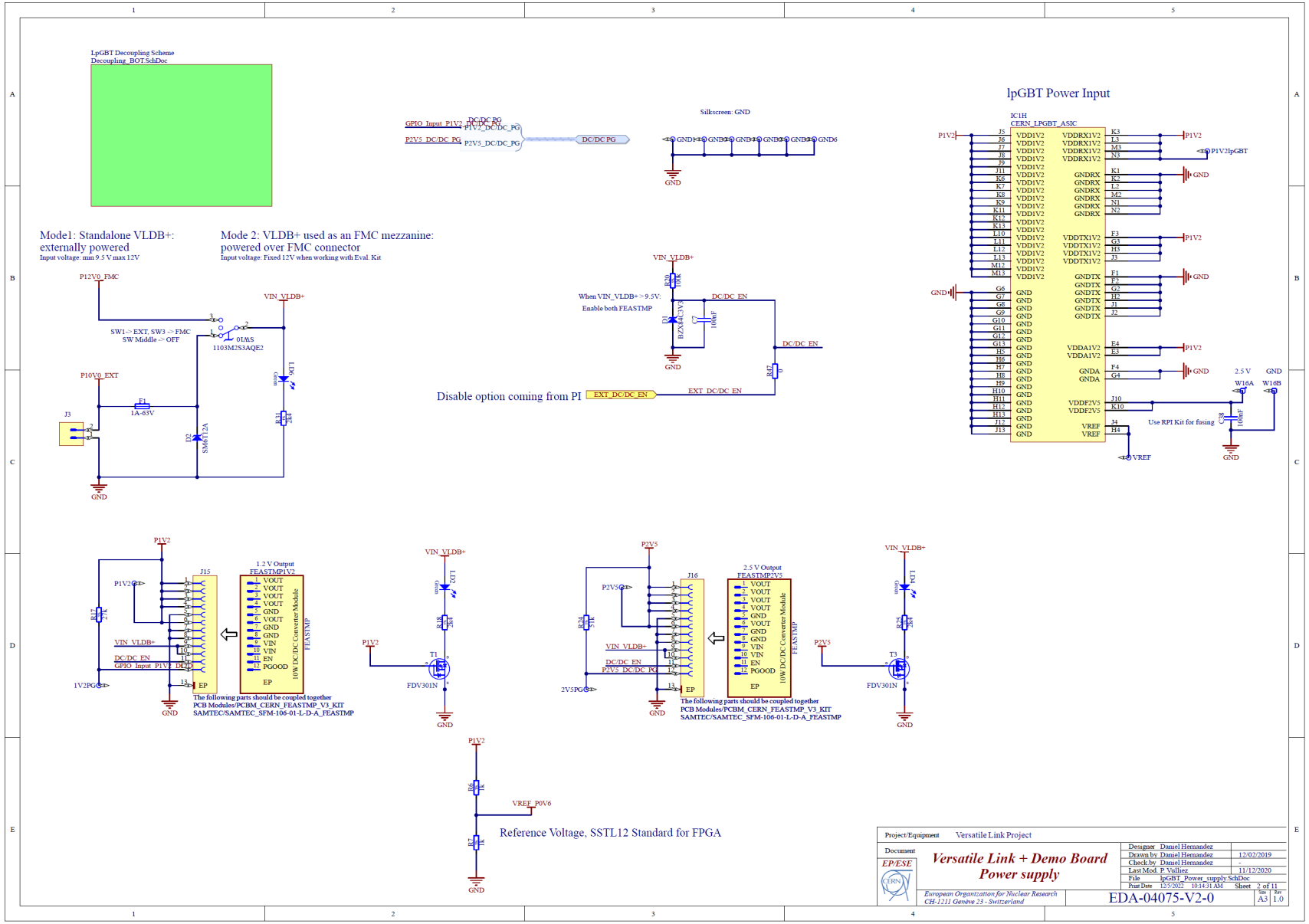

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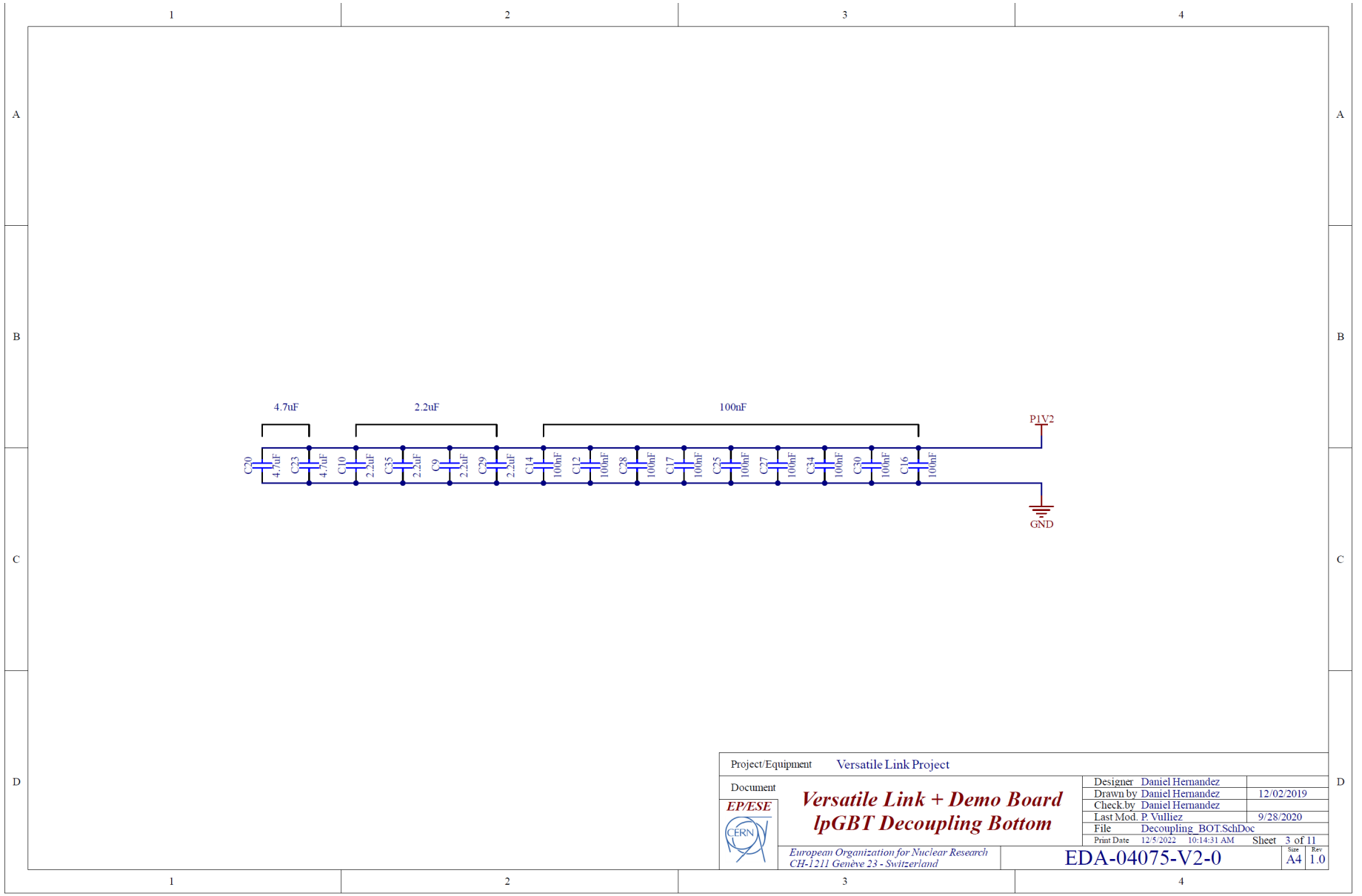

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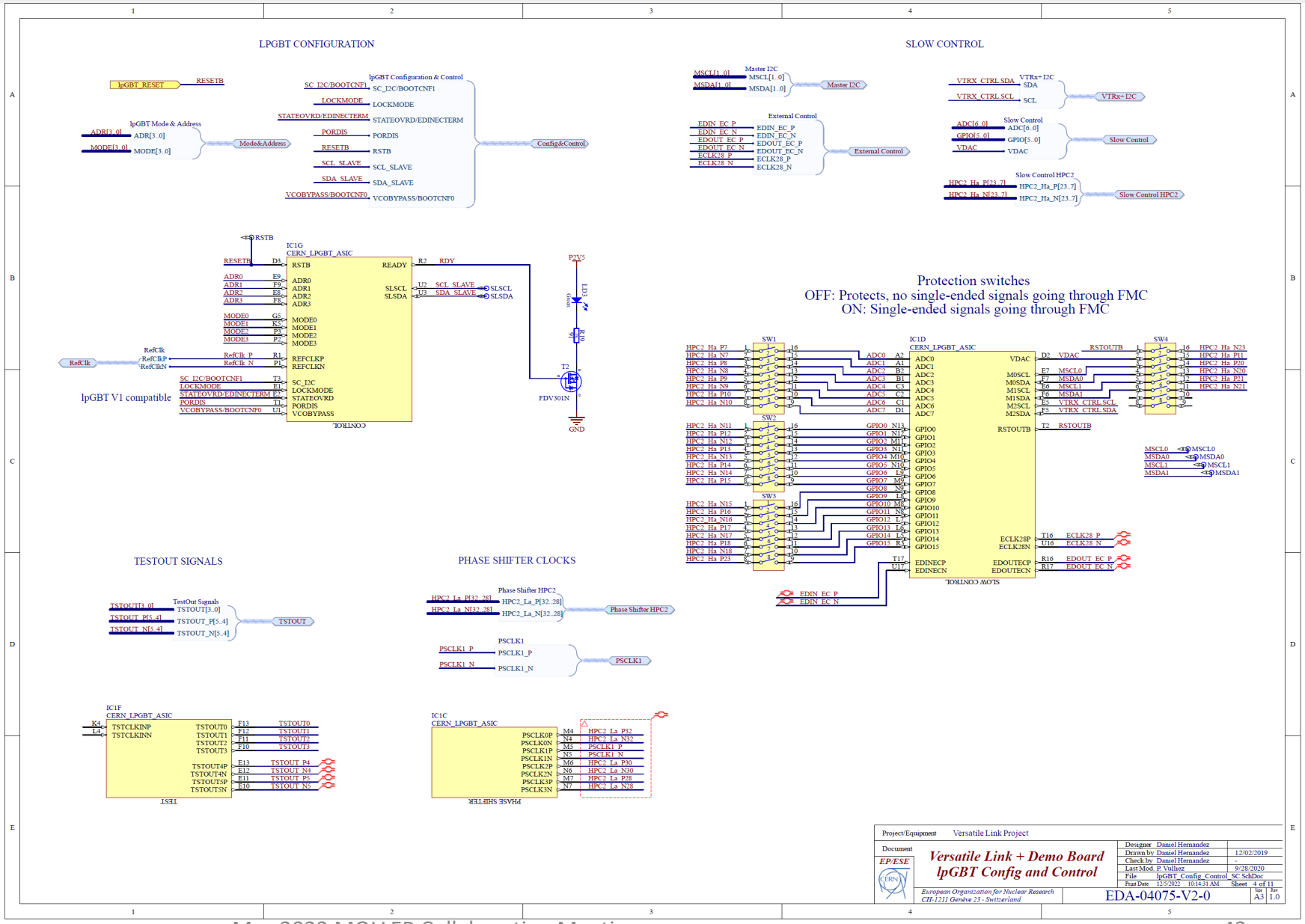

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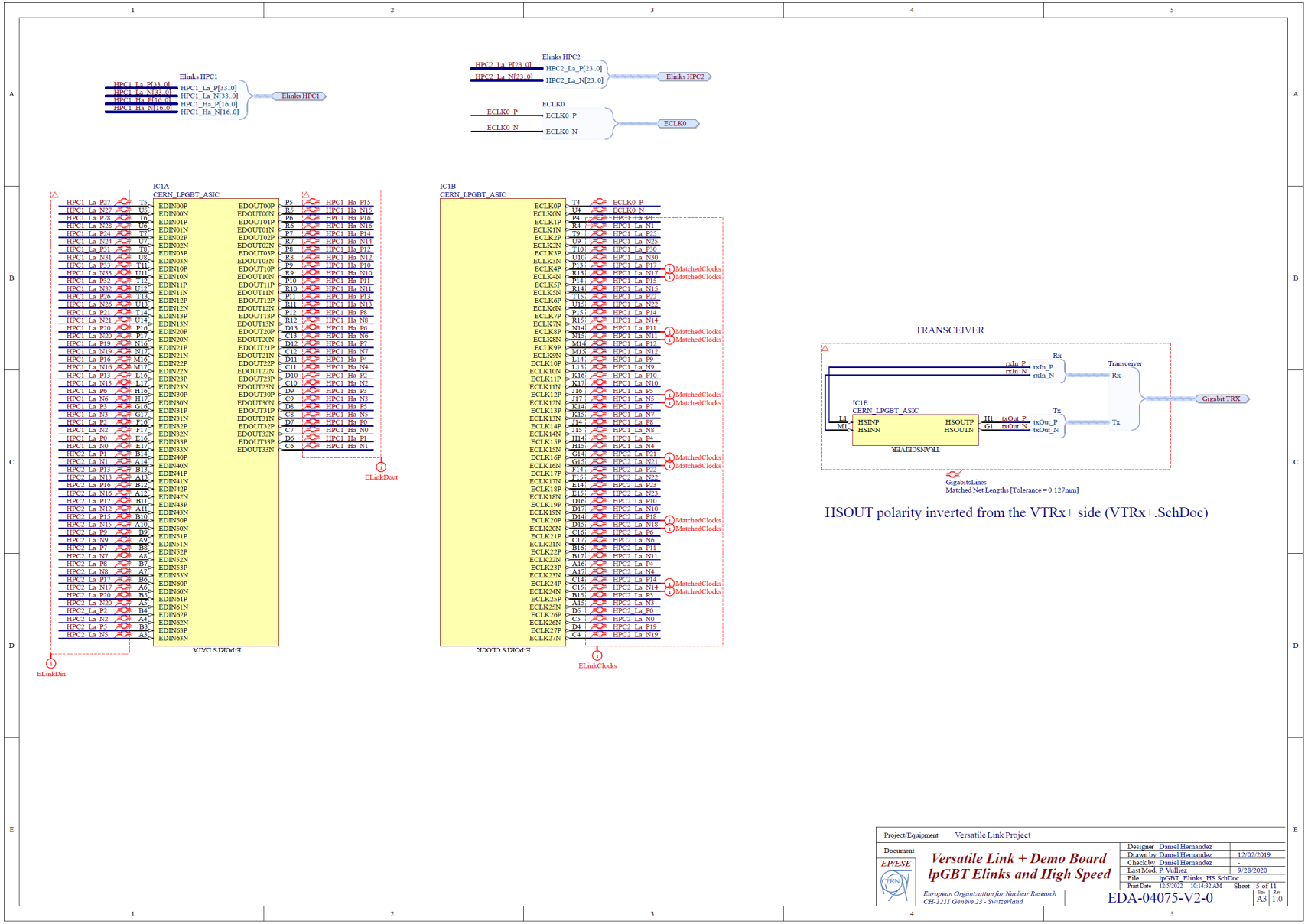

HSOUT polarity inverted from the VTRx+ side (VTRx+.SchDoc)

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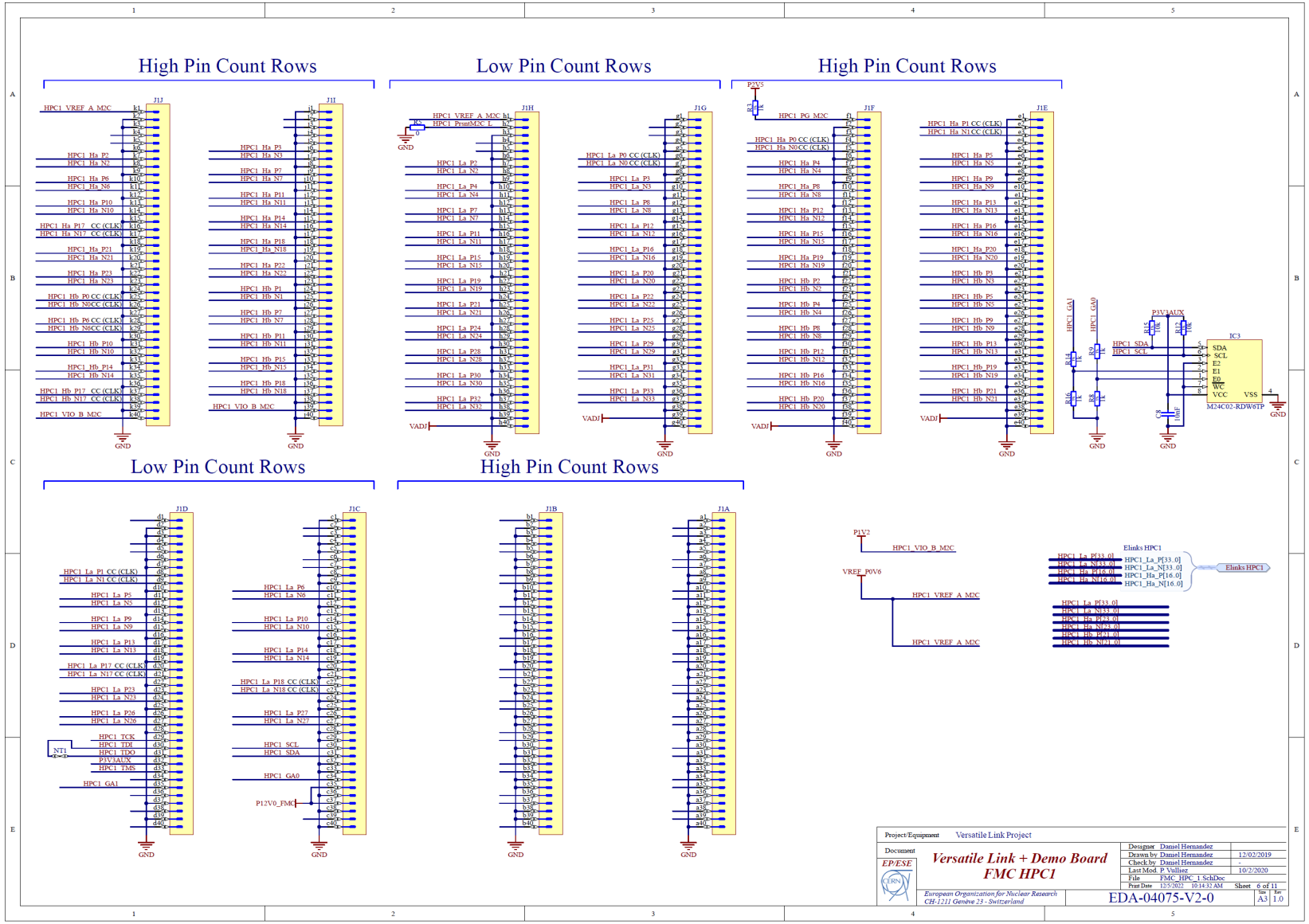
CERN Prototype Board Schematics



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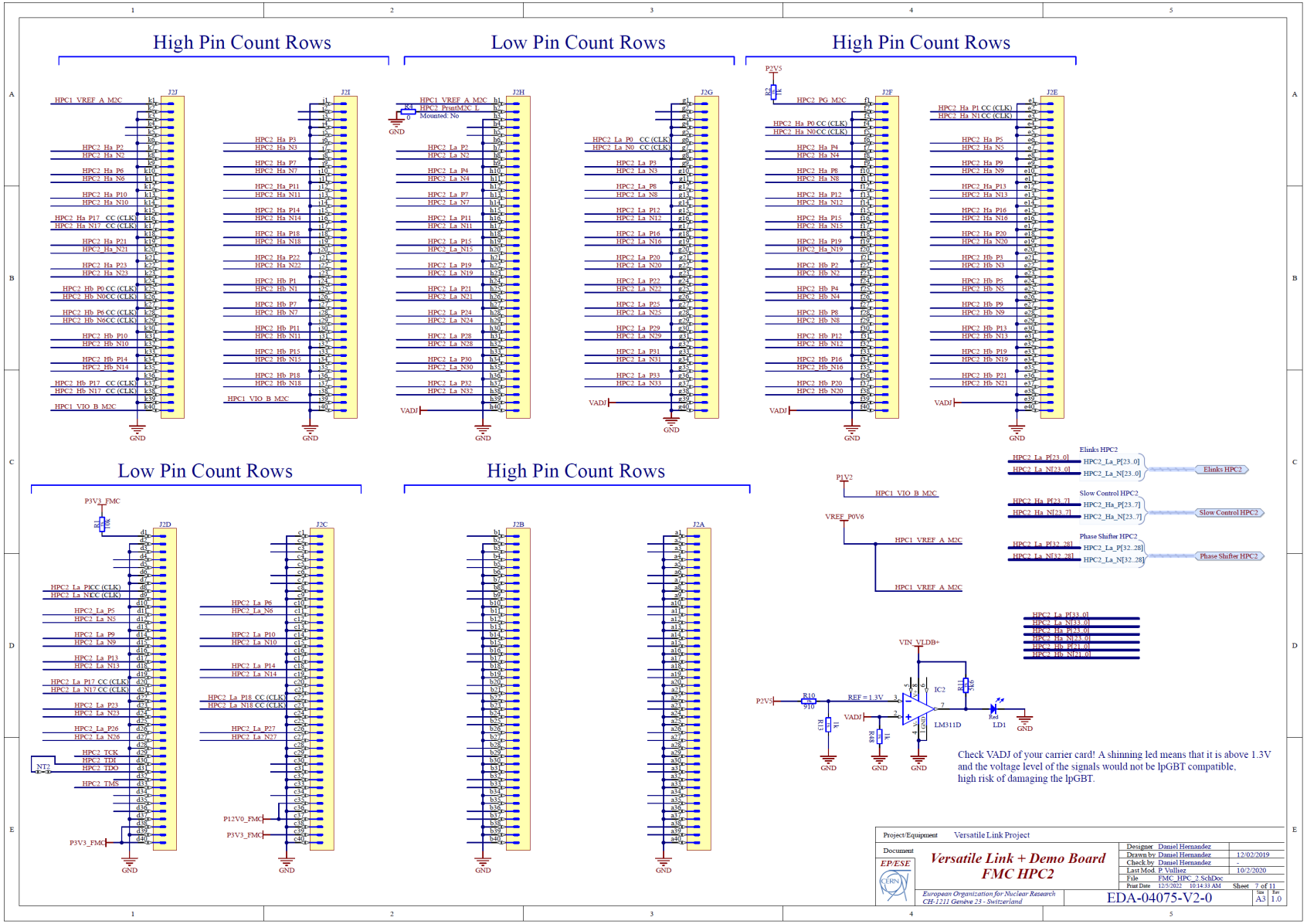

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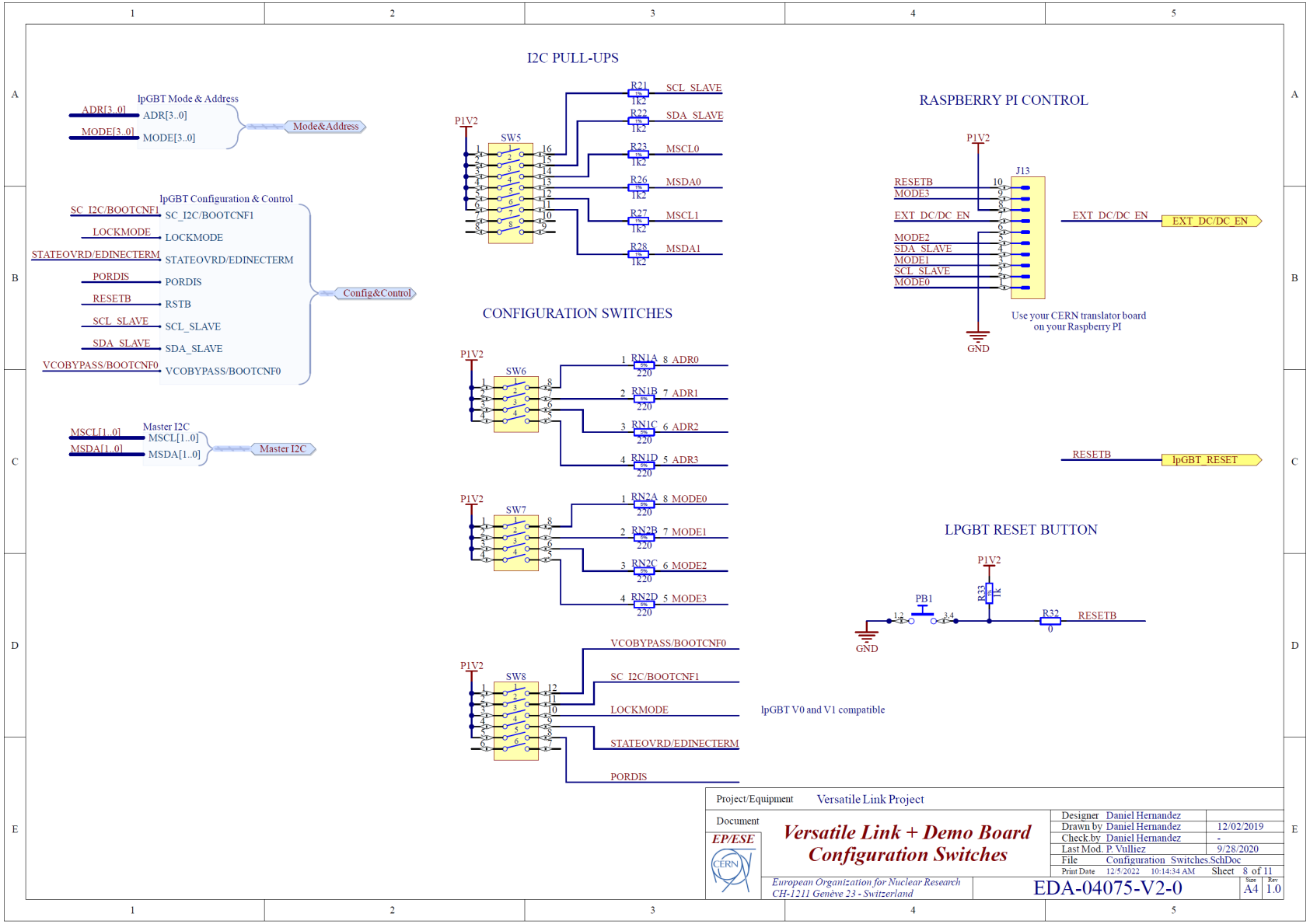

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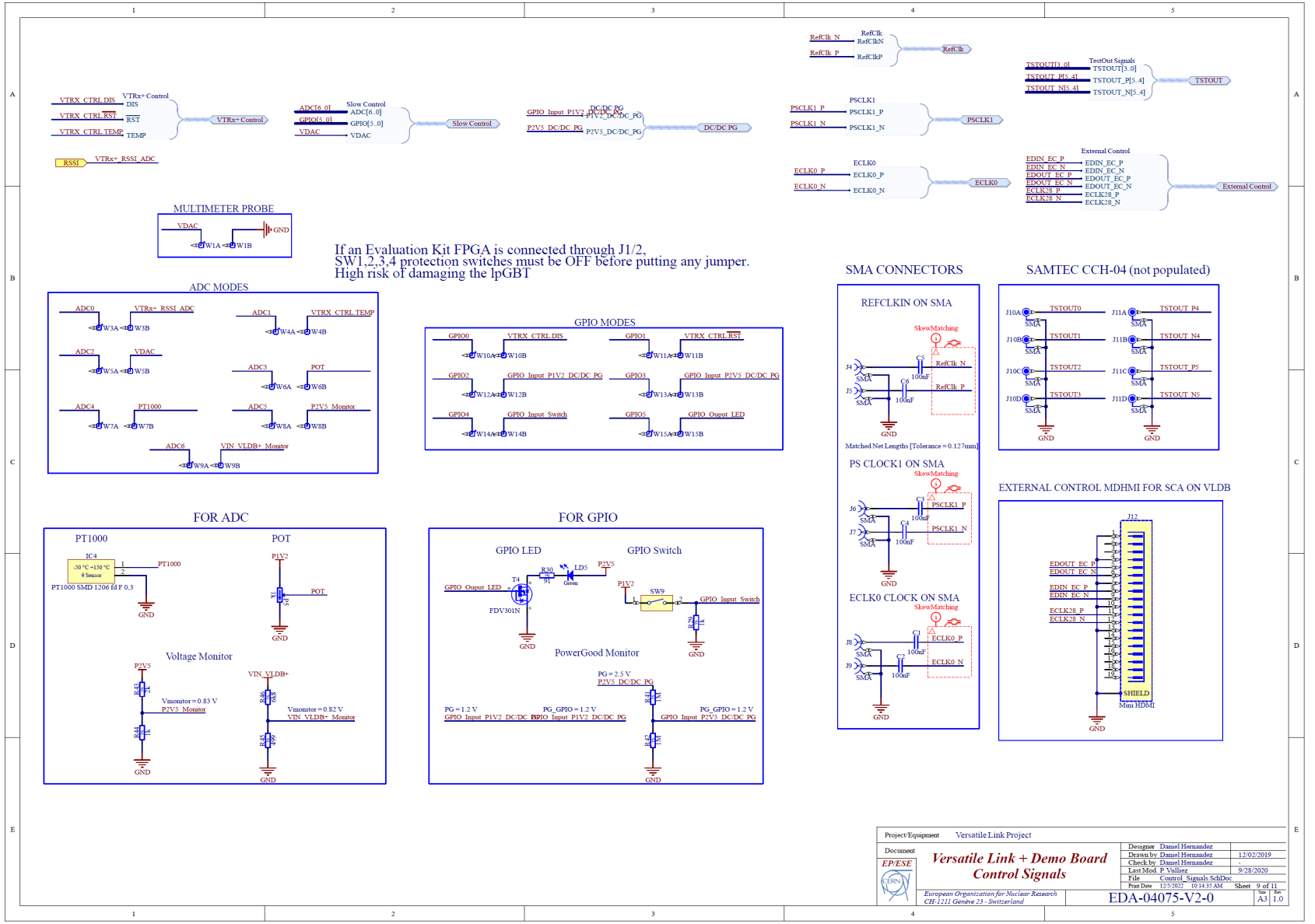

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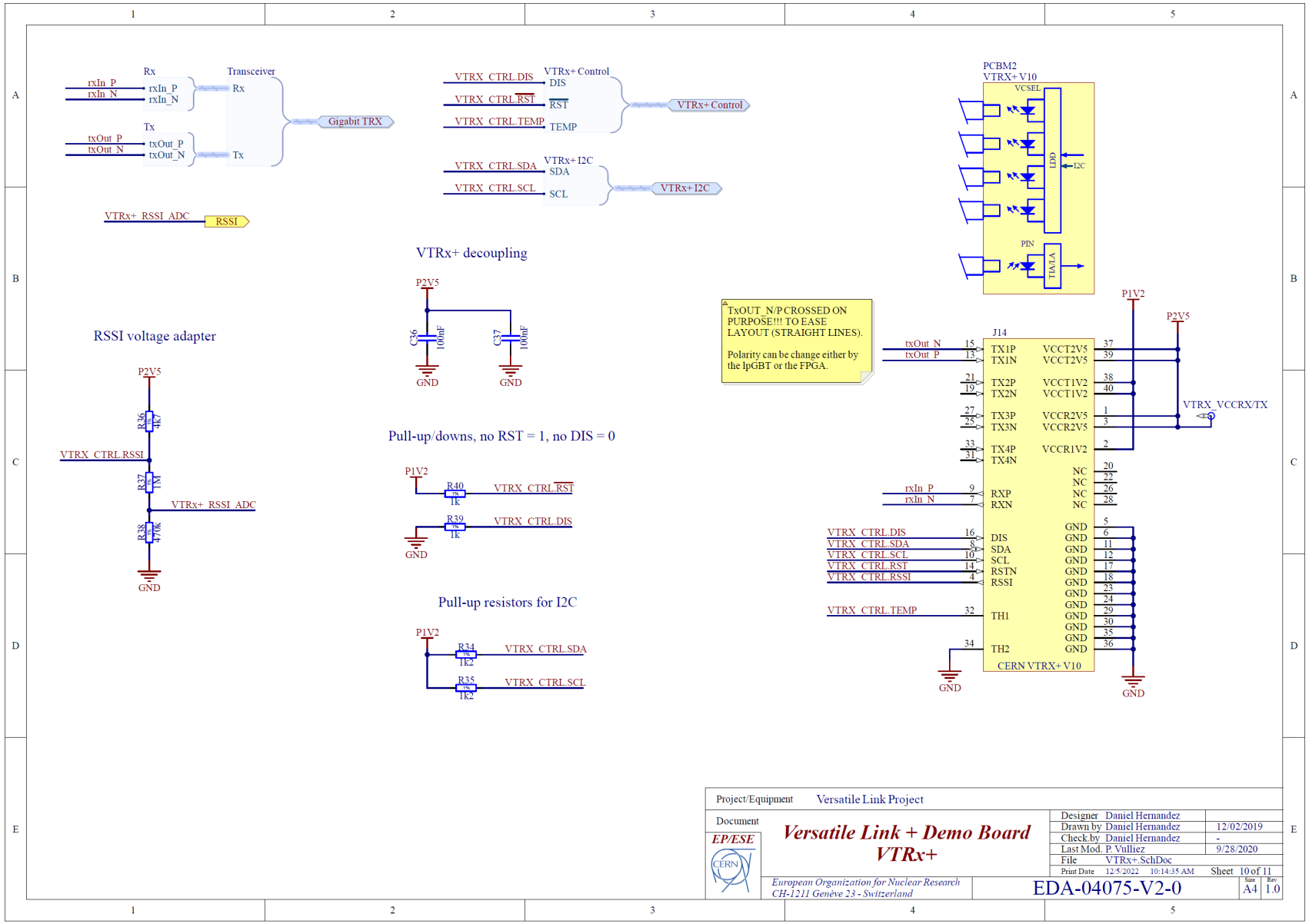

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