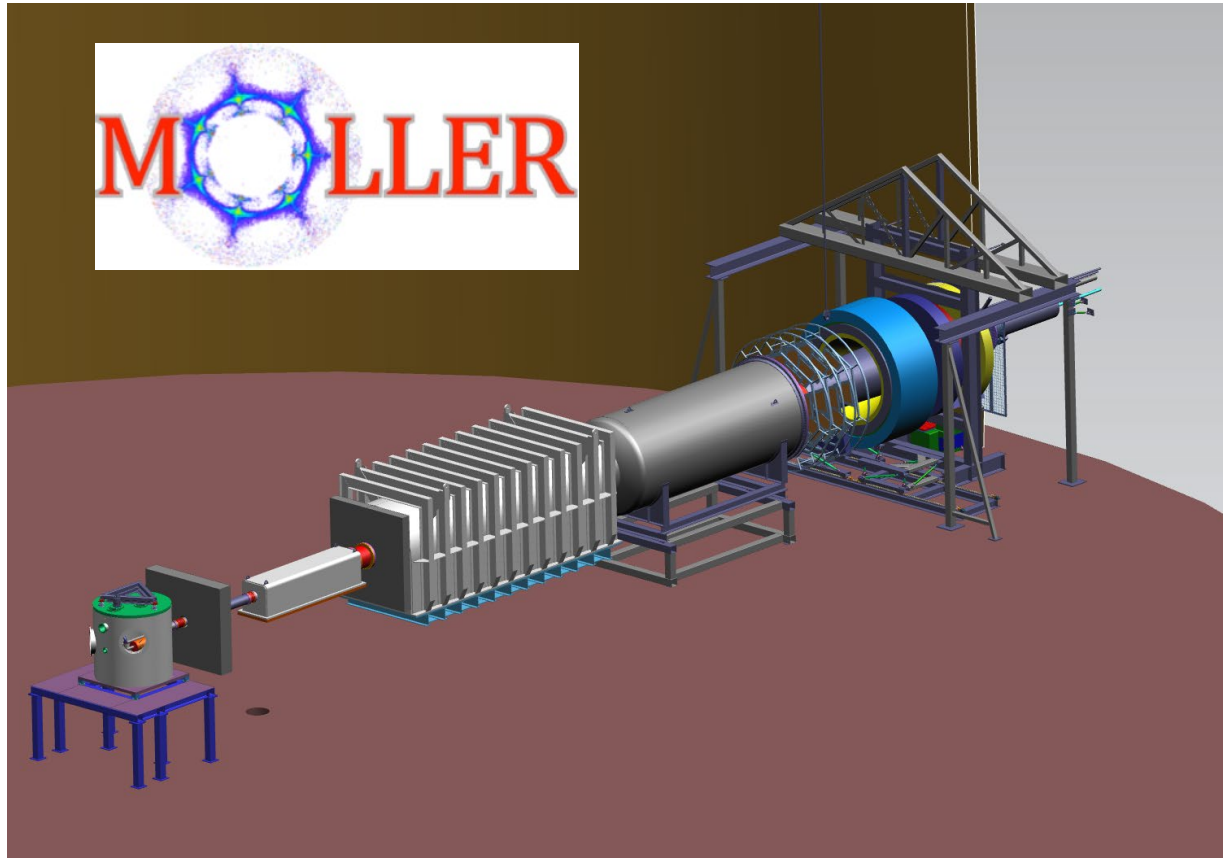
DAQ update

Integration and counting mode DAQ planning for MOLLER (WBS 1.07, 2.07, 3.07)

MOLLER Collaboration meeting, 5-6 May 2023



OHIO UNIVERSITY

Paul M. King – Ohio University

MIE WBS1.07 Level 2 Technical Lead

Jefferson Lab

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JSA

DAQ development contributors

- Common members in all groups
  - R. Michaels, B. Moffit, C. Zorn; JLab
  - B. Blaikie, M. Gericke, J. Pan; University of Manitoba
  - D. McNulty; Idaho State University
  - P. King; Ohio University
- Integration mode
  - D. Bishop, B. Shaw; TRIUMF
  - C. Cuevas, W. Gu; JLab
- Counting mode
  - D. Armstrong; W&M
  - S. Chatterjee, C. Ghosh, H. Liu; U. Mass.
- Digital BCM
  - J. Arrington, Y. Kolomensky, S. Li, Y. Mei, E. Sichtermann; LBNL
  - W. Gu; JLab

Developments since June 2022

- Completed the Final Design Review in December 2022
- Continuing development and testing of integrating ADC
- Tested the trigger distribution plan for synchronizing INJ and Hall readout
- Identified location for GEM MPD crates
- Planning for beamline readout
- Developed plan for including HVMAPS in both integrating and counting DAQ
- Reconsideration of data footprint
- Not much progress on analysis → needs to shift to high priority

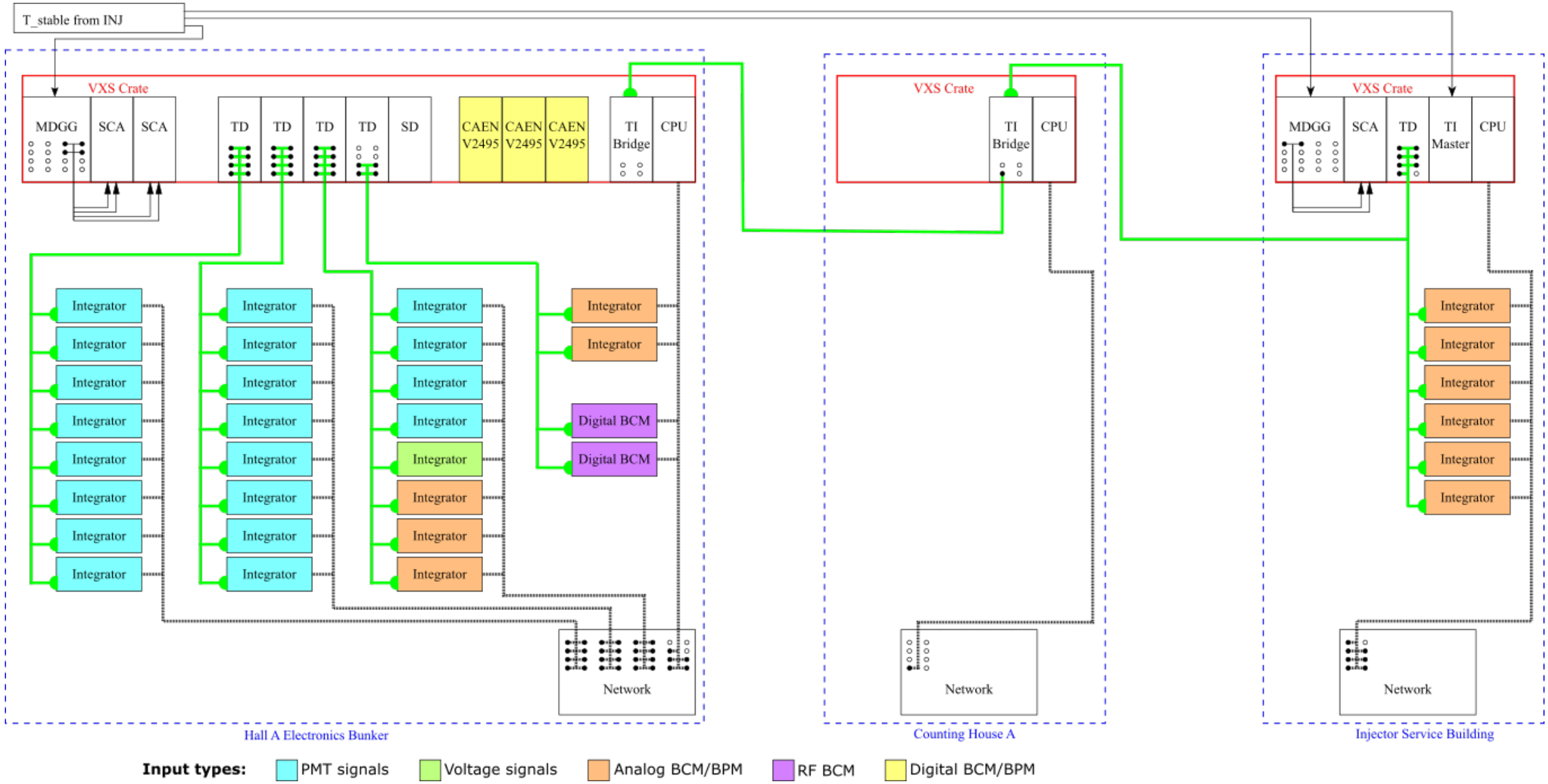
Recommendations from the PDR and actions taken

- Continue plans for reviews of circuit board designs with Jefferson Lab staff before release of production versions.
  - JLab staff have been actively involved in development of the integrating ADC module; W. Gu recently conducted a review for FEG of the DAQ plans
- Update/verify existing electrical/grounding system drawings for Hall A to include new equipment for MOLLER detector and magnet apparatus.
  - The collaboration has a Grounding task force that will complete its work soon, including updating the existing Hall A grounding system drawings.
- Carefully review the requirements for new fiber optic cables from the Injector Service Building (ISB) to the Hall A electronics bunker locations and create an installation plan.
  - Contract to install the ISB-CHA fiber has been put in place to be done in this SAD; CHA-Hall fiber installation planned for the MOLLER assembly period.
- Make progress on the prototyping of the Integration/readout board a priority. The more time it can be tested and integrated into the CODA framework the easier it will be to flush out all potential DAQ and timing issues.
  - Prototype ADC module delivered in November to B. Moffit to begin CODA installation

Integrating ADC development

- Full 16-channel prototype tested with beam at Mainz
- ADC board design has undergone preliminary review by JLab staff
- Prototype chassis designed and constructed at JLab
- One module is now with JLab DAQ group for installation of CODA
- Power can be supplied through Power over Ethernet (PoE) or an external 48V supply. Prefer PoE, but to be checked with grounding working group

Integrating DAQ overview



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Bench testing of trigger distribution between ISB and Hall

TriggerGeneration (Timaster(slot#3))

↓ OpticFiber, SingleMode, 1500 ft

TriggerBridge (TI_bridge_supervisor (slot#6))

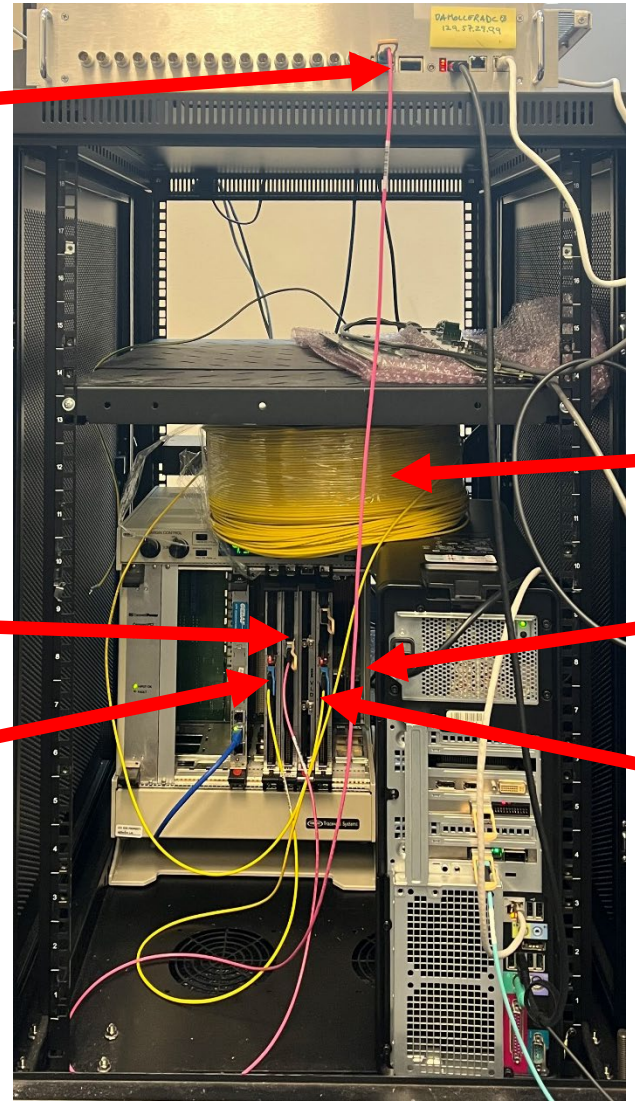
↓ fake_SD backplane

TD (TD (slot#4))

↓ OpticFiber, MultiMode, 6ft

Integrating ADC (TInode) in hallA

Integrating ADC (TInode) in the Injector Building (when the second ADC is available)

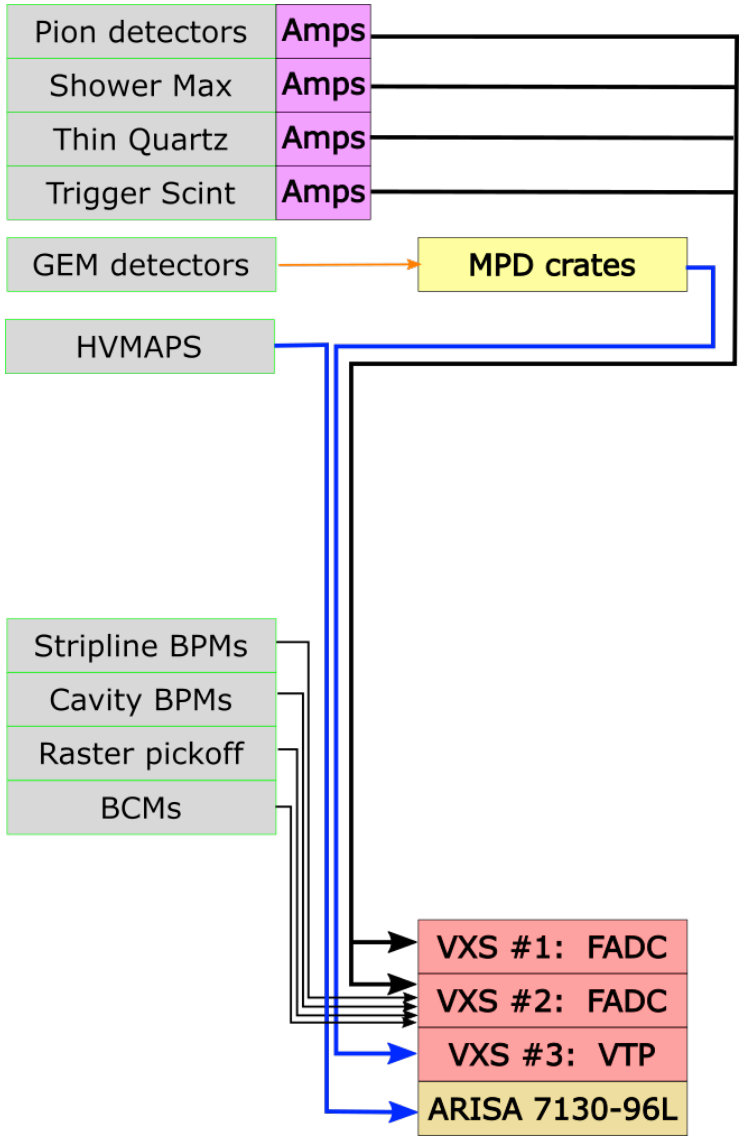


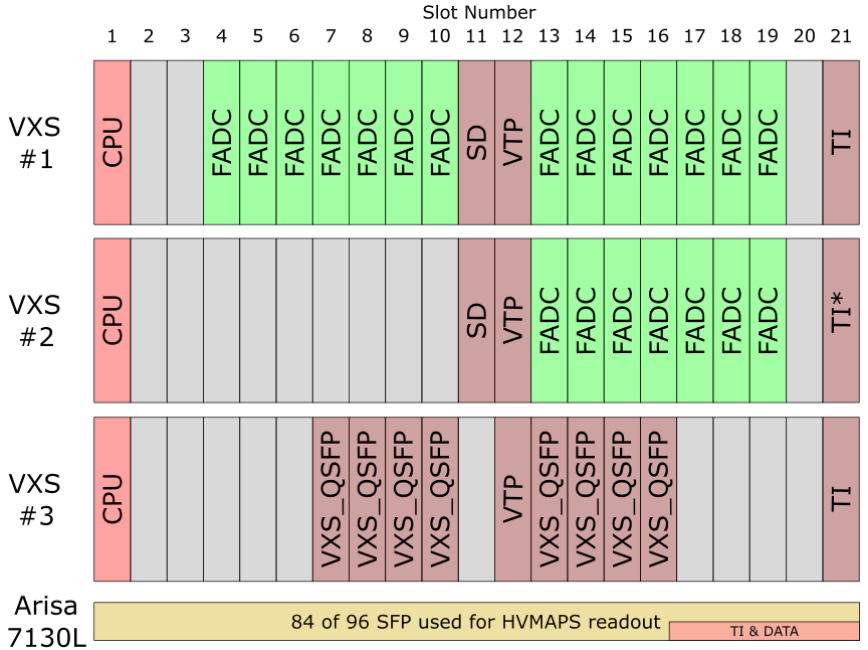
Picture and description, courtesy of W. Gu

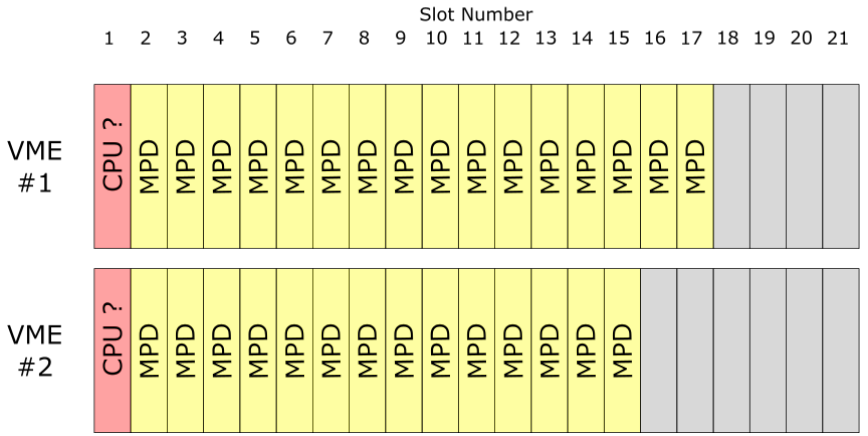
Testing and development needed to complete the ADC

- Testing of the TI interface on the ADC board with TIpice
  - —In progress
- Installing Linux and porting CODA to the Ultrascale+ on an evaluation board
  - —Done
- Install Linux/CODA on the SOC on the ADC
  - —Done
- Decide if ground isolation using PoE++ is acceptable or should use independent isolated power supplies
- FPGA firmware development to form the helicity window quantities
- FPGA firmware development for streaming of all samples
- Development of Linux driver to access the FPGA result registers
- CODA ROLs
- Testing

Subsystem overview: counting DAQ

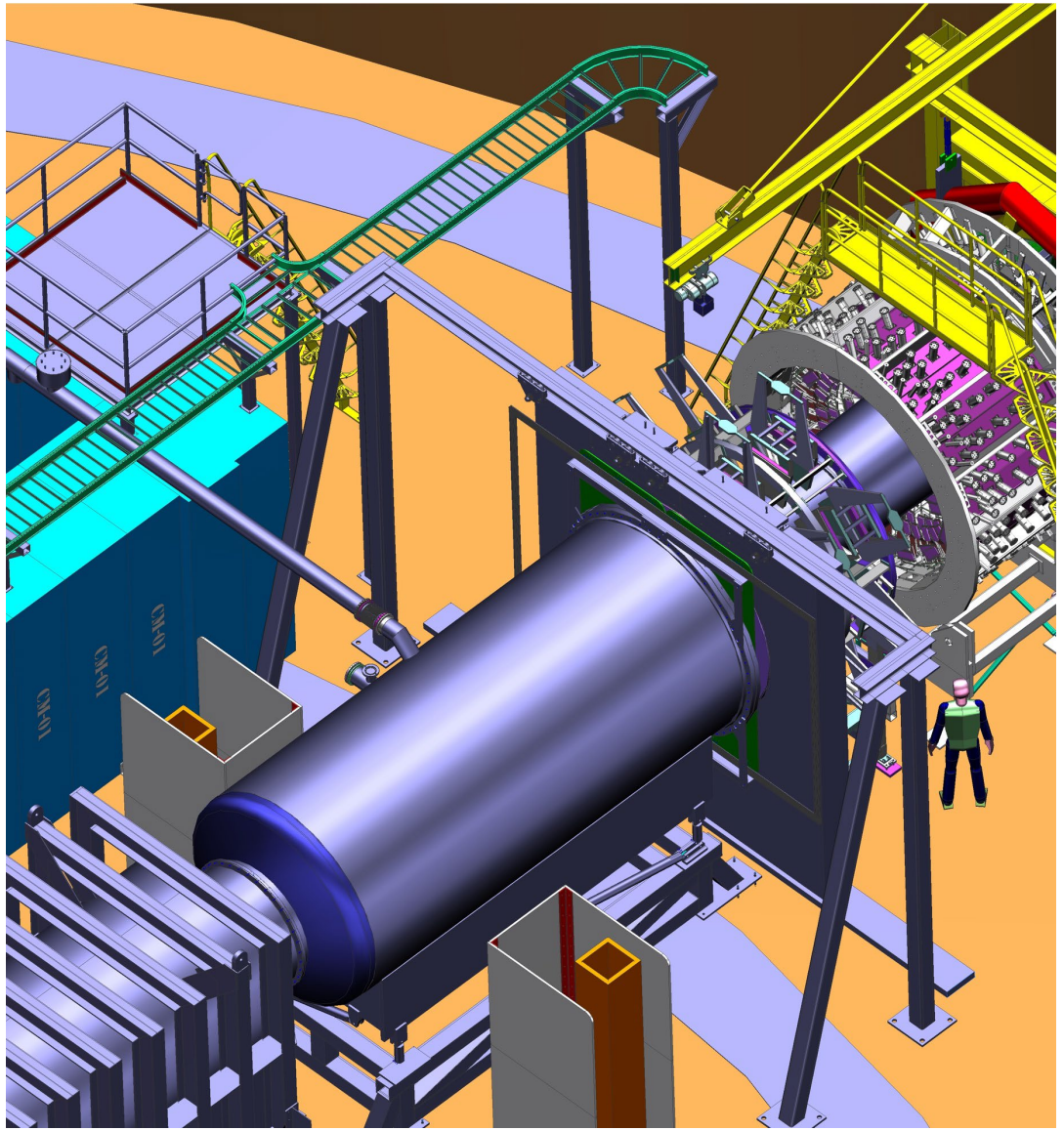






GEM Readout Planning

- GEM modules will be instrumented by APV25 cards, which will be connected to MPD modules via HDMI cables
- Data from MPD modules will be transferred over optical cable to a VTP module
  - This is identical to the system currently in use by the SBS experiment
- MPD modules will be in shielded area near the detectors
  - Simulated total dose over the full experiment is a few krad
  - We are in communication with SBS to understand their radiation experience with the MPDs
  - To date, no APV or MPD failures have been attributed to radiation



Beam monitor readouts

- All JLab BCM and BPM receivers have analog outputs which can go to ADCs
- Would prefer digital readout; development underway for Hall A/C experiments

Planned Readout of Digital Data for Beam Monitors

https://userweb.jlab.org/~rom/digibcm

J. Musson's electronics

CAEN V2495 PLU

Beam Monitor Electronics

beam current (BCM) or beam position (BPM) Digital data

Fiber

Electronics that sums the data in each integration window and can be read out by the DAQ

Integration gate
4 usec to ~1 hour

John Musson
Chad Seaton
Bob Michaels
Randall McClellan (initial version)

- UC Berkeley and LBNL are developing a digital BCM receiver
  - The input bandwidth is closer to the integrated PMT channels
  - Trigger Interface connection and readout would be done through QSFP as for the integrating ADCs

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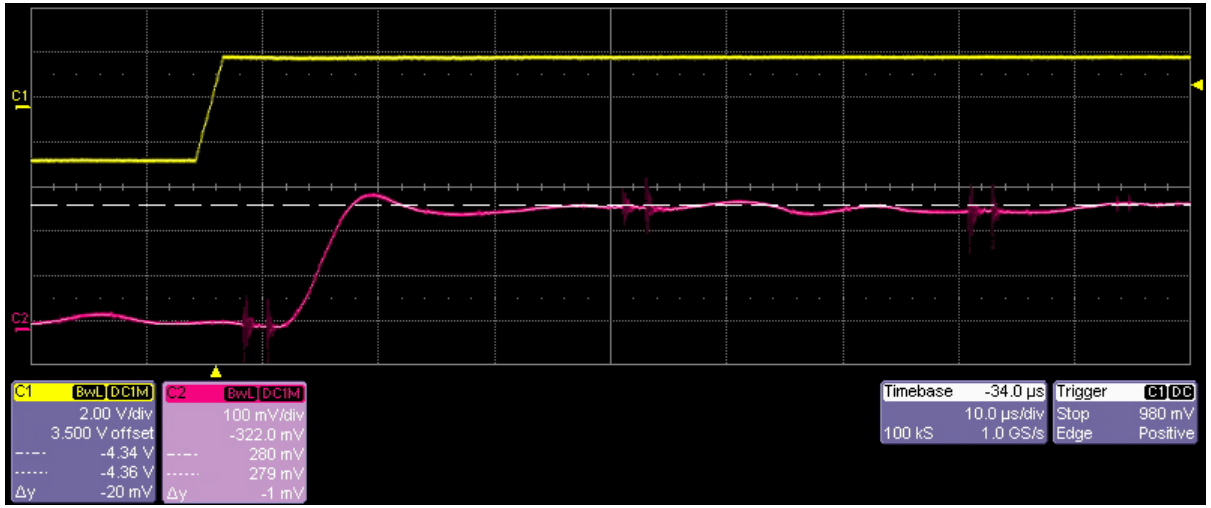
Bandwidth and latency considerations for beamline readout

- We have sent a BPM and BCM requirements document to N. Rider
  - Highlighted the bandwidth and timing requirements to match with the detector signals

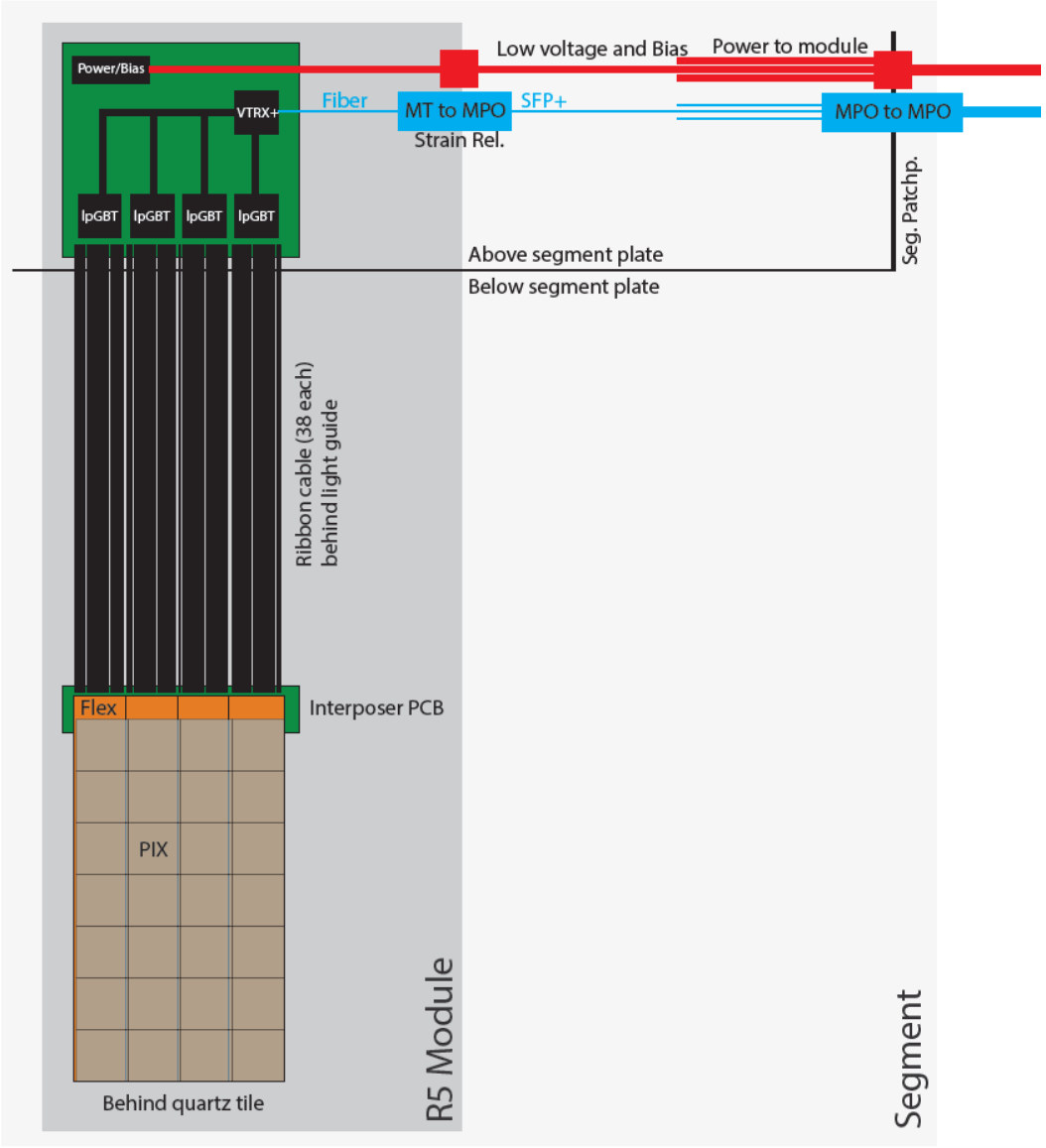
Bench test of BCM digital receiver, showing latency.
Courtesy of J. Musson



- JLab SEE electronics
  - Bandwidth of analog output signals is ~30kHz
- JLab digital receivers
  - Digital sample rate is 1Msps, allowing a maximum bandwidth of 500 kHz
  - Analog output (18-bit DAC) signals have a filter with effective bandwidth of 100-200 kHz
- For both the JLab SEE and digital receivers, the analog outputs have a few µs latency compared to the inputs. We will allow for this by adjusting the integrating ADC gate timing.

HVMAPS

- Each Ring-5 tile would have 28 HVMAPS chips
- Readout from HVMAPS done via low power gigabit transceiver (lpGBT) SER/DES chip and the VTRx optical transceiver
  - One lpGBT supports 7 HVMAPS; four lpGBT supported by one VTRx
  - VTRx output is SFP+ fiber
- Data from HVMAPS collected in FPGA-based Arista switch (Arisa 7130 96L)
  - This will also have a TI connection to allow CODA integration
- HVMAPS will be part of counting mode DAQ; will be operated independently during integration mode running



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HVMAPS Operation goals

Counting mode

- Pixels are self triggered, and send their hit data and timestamp over the fiber connection
- FPGA on Arisa switch uses timestamps to associate HVMAPS pixel hits to triggered event
- Fairly loose requirement to match timestamps to trigger due to 25 ns time binning on GEMs
- Pixel hit data is send to CODA data stream to allow combined analysis with GEM tracks

Integrating mode

- Run as independent data stream to generate an occupancy map
- HVMAPS are run in a triggered mode, to just record being hit within a narrow trigger window (~10 ns)
- All hit pixels are read over the fiber and accumulated to form a 2D occupancy map

Data rate, file segment sizes, and data set size

- The standard data rate for the integrating DAQ will be about 130 MB/s
  - One hour of data would be about 470 GB
- A convenient size for the data file segments might be 20 GB → ~150 seconds
  - Hour-long runs would be split into about 23 segments
- Many file segments makes it easy to run analysis jobs in parallel, but short file segments may make it harder to recognize and cut out beam trips or other instabilities

- The total data footprint has been recalculated in DocDB#1027; total is 14PB
  - Production + Compton raw data: 9.5PB (main production DAQ, 7PB; HVMAPS, 0.5PB; diagnostics mode, 0.5PB; Compton, 1.5PB)
  - Production + Compton analysis results: 2PB
  - Tracking raw data & analysis results: 1.5PB (raw data, 1.25PB; analysis results, 0.25 PB)
  - Simulation: 1PB

Mock-data and analysis testing

- Mock-data generator within “japan” creates realistic data files with time-dependent and randomized generation of beam parameters and detector signals, including correlations
- First model of the integrating ADC data-structure has been added; should be updated as we become familiar with the actual data stream
- Analysis of these data files allows testing of throughput and processing algorithms
  - Processing time for initial mock-data (216 PMT channels and 50 beamline channels) is ~5ms per event; this is faster than we had expected from scaling arguments
- We should restart the parity analysis group discussions
  - Starting point is the japan framework as used in PREX/CREX; should revisit what worked well and what was missing
  - Are there reasons to make major framework changes, or even start with new framework?
- For tracking analysis, expect to look at what can be used from SBS analysis

Paul King

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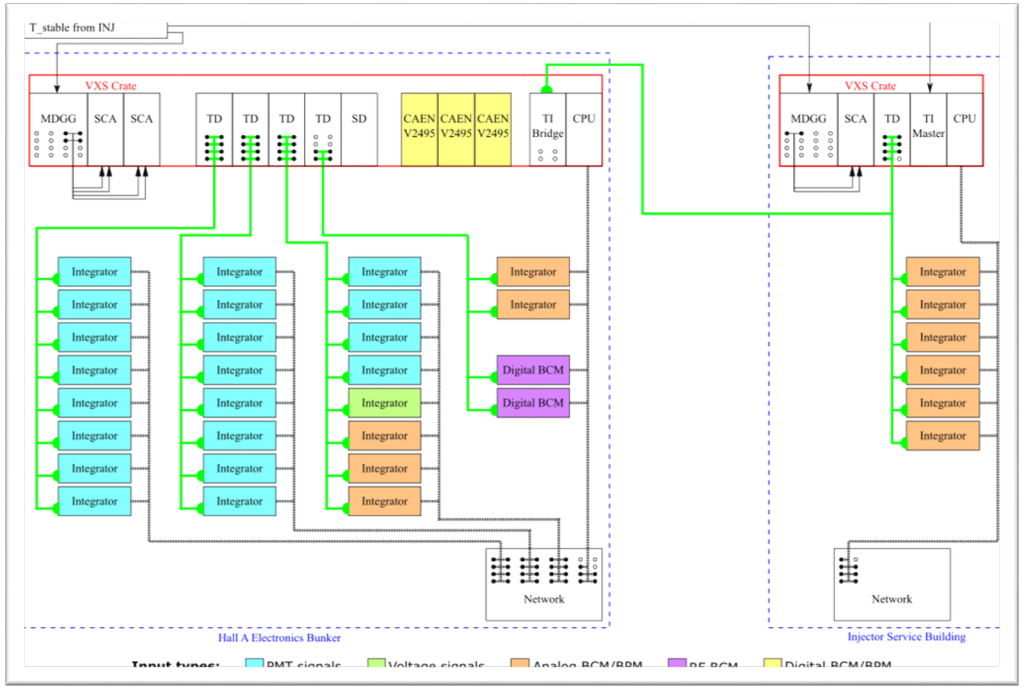
Summary

- Integrating and counting DAQ working groups are preparing for procurements to begin shortly
- CODA development for integrating ADC is continuing
- Bench testing of JLab digital beam readout has started
- Objective is to start “subsystem testing” this fall, and complete the bulk of “full system testing” by May 2024



Backup slides

Draft plans for integrating mode functionality

- ADC sample clock will run at 14.7 MHz (250 MHz/17)
  - If a lower sample rate is desired, we would keep the clock the same and discard samples within the FPGA
  - Input bandwidth is ~1MHz, so need to keep effective sample rate > 2 MHz to avoid aliasing
- Main mode: accumulate over the helicity window and four equal-length sub-blocks
  - 32-bit values of sum, sum-of-squares, min, max, and number of samples reported for each block. Data rate from 32 modules 130MB/s for full window + 4 subblocks
- Waveform mode: all samples are reported
  - For Fourier analysis, need to be able to get all samples from about 1 continuous second
  - For evaluation of noise in helicity window, need samples within helicity window (and possibly also the T_settle period)
  - The densest packing for waveform data would be ~34 MB/s/channel. This is presumed to be used infrequently and is not included in the data rate or data set calculations

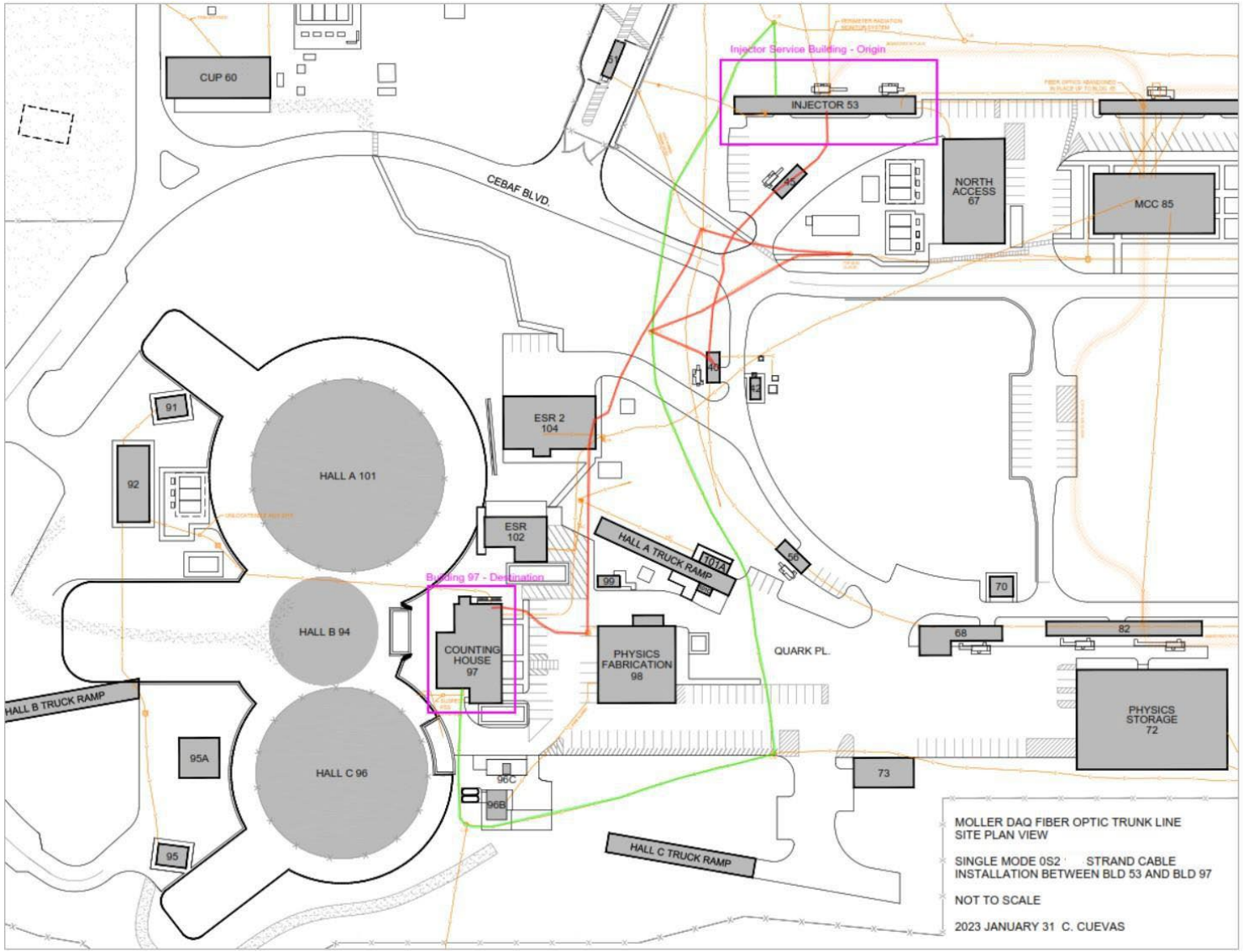
Integration mode channels

- Detector array (280 total)
  - 224 Main detectors, 28 shower-max detectors, 28 pion detectors
- SAMs, LAMs, and beamline (233 channels)
  - SAMs: 8
  - LAMs and diffuse background monitors: 28 (14 LAM + 14 DBM)
  - Injector beamline: 96
  - Transport line and Hall beamline: 87 (PREX/CREX used 64; my count so far ~77 ch.)
    - Channels needed for beamline may be lower due to LBNL & JLab digital recievers
- Scanner (6+7 channels)
  - X/Y scanner: 2 PMTs + 2 position voltages (positions might go into a FADC or VQWK?)
  - Linear scanners: 4 PMTs + 4 position voltages
  - Reference voltage for positions
- Total: 512 channels → 32 16-channel modules
- HVMAPS & Digital BCM expect to connect into CODA in same way as ADCs

Proposed plan to add the fiber connection

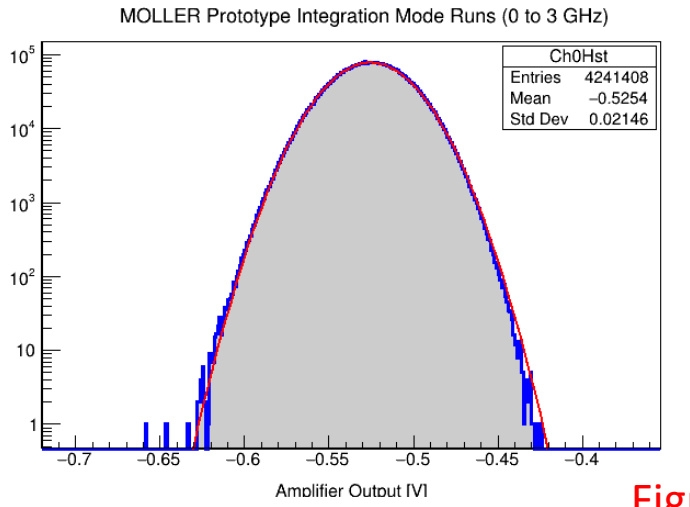
- ISB to CHA
  - 1550 linear feet of armored fiber (48 fiber cable, single mode fiber)
  - Ohio U would contract with an external vendor (selected and coordinated by C. Cuevas) to have the fiber installed during this SAD
- CHA to Hall A DAQ shieldhouse
  - 500 linear feet of armored fiber (48 fiber cable, single mode fiber)
  - Fiber and installation would be added as part of Infrastructure WBS, and would be done during MOLLER assembly period

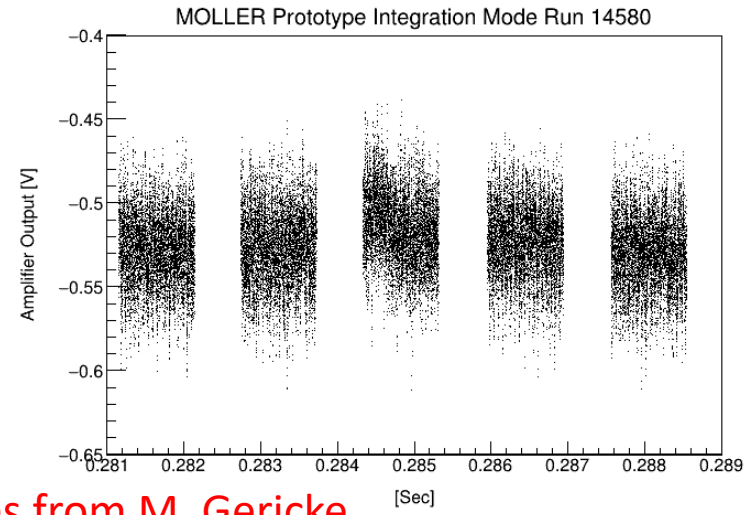
Fiber path

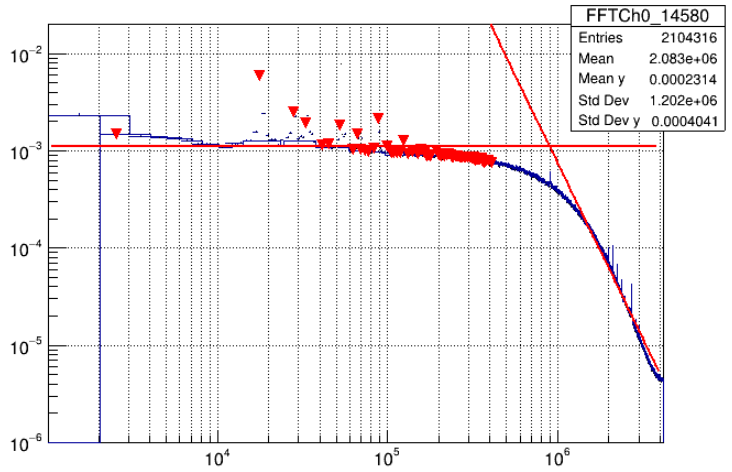

Injector Service Building - Origin
INJECTOR 53
CUP 60
CEBAF BLVD.
NORTH ACCESS 67
MCC 85
ESR 2 104
HALL A 101
91
92
ESR 102
HALL A TRUCK RAMP
101A
99
70
Building 97 - Destination
HALL B 94
COUNTING HOUSE 97
PHYSICS FABRICATION 98
QUARK PL.
68
82
HALL B TRUCK RAMP
PHYSICS STORAGE 72
95A
HALL C 96
96C
96B
73
95
HALL C TRUCK RAMP
MOLLER DAQ FIBER OPTIC TRUNK LINE
SITE PLAN VIEW
SINGLE MODE 0S2 STRAND CABLE
INSTALLATION BETWEEN BLD 53 AND BLD 97
NOT TO SCALE
2023 JANUARY 31 C. CUEVAS

Results from the integrator ADC during 2021 Mainz tests

- The integrating signal level is gaussian except for beam excursions
- The beam test firmware gave 8191 samples over $\simeq 0.983\ ms$ with about $\simeq 0.5\ ms$ break between sample – next version goes up to full sampling rate at $\simeq 15\ Msps$
- The high sampling rate we chose for the ADC is a good feature, as it allows us to run DFTs in diagnostic mode and identify potentially troubling noise sources and beam problems.

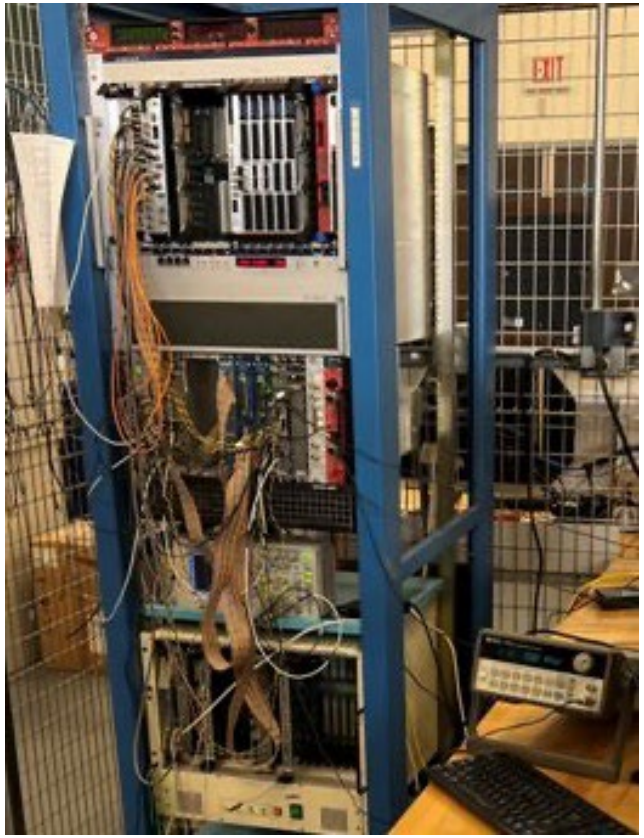




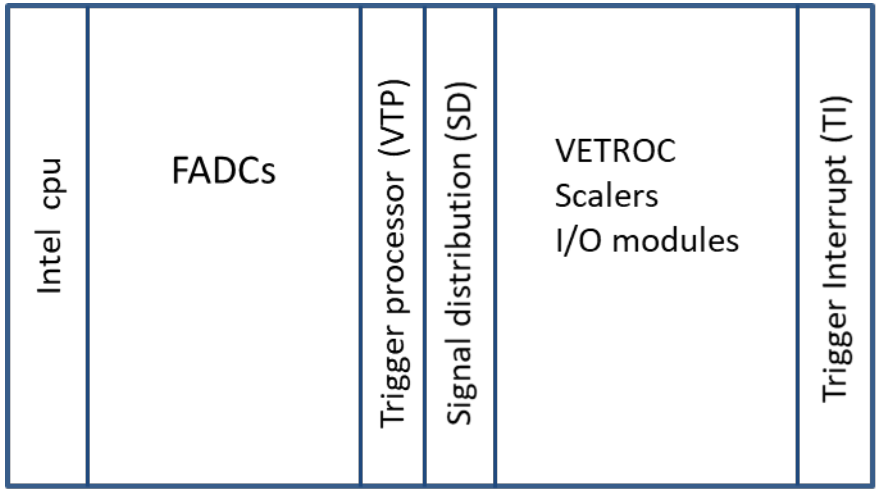


Figures from M. Gericke

Counting Mode Test Stand



- Test stand in TEDF used for common development of counting mode, Compton polarimeter, and Moller polarimeter DAQ systems
  - DAQ designs share same concept: FPGA in VTP collects data from front-end (FADCs or VETROC) to form event triggers
- Development objective for counting mode: VTP firmware to trigger on FADCs of single elements (quartz tiles) or two-channel coincidences (trigger scintillator)



Response to FDR committee about experience with GEMs in SBS

We want to make sure the DAQ talks tomorrow cover issues experienced in SBS with readout used for their GEM system.

- SBS uses GEMs in both BB and SBS using the APV→MPD→VTP readout chain
- A lot of the stability issues at the start of GMn were resolved with various firmware updates both to the VTP and MPDs.
- The big limitation, as seen by SBS, is the transfer of data from MPDs to VTPs and from VTPs to network
- Remaining instability issues now generally occur for various reasons when an APV misses a trigger.
  - Bryan and Ben have added diagnostics to tell which APV or which MPD is causing the problem, and there are procedures to power cycle the MPD crates, VTP crates, or the low voltage to the APV card. This usually can fix any APV issue that is not a physical cabling or disconnect problem, and they continue to gain experience with this.
  - They also have configurations in which problematic APVs can be disabled
- The BB GEMs occasionally cause DAQ issues at the start of run in our current running (just needs a reset most of the time), and the SBS GEMs cause problems at about the same rate x2-3 or so due to the larger number of channels
  - This is roughly 1 or 2 issues in 1-2 shift days for the BB GEMs
- The INFN GEM layers are the only ones that are still having issues right now, but these have a different design than the other layers, and they think the problem has something to do with the low voltage configuration

Response to FDR committee about experience with GEMs in SBS, pt2

- MPD data transfer links are 1.25 Gb/s and VTP output link is 10 Gb/s
- MOLLER (280 APV, 28 MPD) is similar in size to BB (328 APV, 24 MPD) but expects lower data rates
  - Most of SBS MPD cards readout 15 APV, but MOLLER will have 10 APV per MPD, so the data rate from a typical MPD will be 2/3 of SBS's at the same rate and number of samples
  - In order to saturate the VTP 10GbE link after zero suppression with 5kHz event rate, MOLLER would need to have GEM occupancies of ~58%; we expect 5-10% at 100nA, and can reduce beam current or prescale triggers if needed
- MOLLER will benefit from the continuing development of the APV→MPD→VTP readout chain during SBS
- MOLLER's design already incorporates one lesson from SBS: using more MPDs than the minimum decreases transfer time by having more links

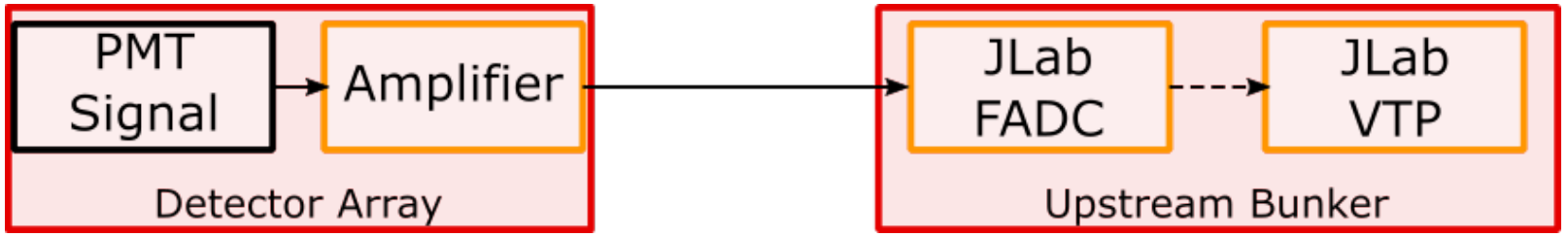
ARISA 7130 96LS

- 7130L is multiple devices in one; performing layer 1+ switching in only 5 ns, enabling unrestricted access to an onboard FPGA and containing an x86_64 server.
  - 84 SFP+ ports used by VTRx connections
  - Remaining SFP+ ports can be used for TI connection
- FPGA (UltraScale VU7P-2) plus quadcore x86 CPU
- Development in parallel with Mainz HVMAPS effort

Rack space estimate for DAQ for 40U (70inch) racks

- Integration mode: 71U in Hall, 31U in INJ
  - Integrators, 1U rackmount units, assume +1U for airflow
    - INJ: 6 modules → 12U: 0.3 rack
    - Hall A: 26 modules → 52U: 1.3 racks
  - VME/VXS: 11U height, front to back airflow
    - Trigger distribution in Hall
    - Trigger supervisor in INJ
  - NIM crate: 7U +1U
    - One each in Hall and INJ
  - **Don't have space needs for HVMAPS or digital BCM receivers yet**
  - **Doesn't include integrator power supplies, or the HV and LV supplies**
- Counting mode: 44U in SBS bunker, 22U in downstream doghouses
  - Three VXS crates: 11U each, front to back airflow → 44U
  - Two VME crates in two "doghouses": 11U each, front to back airflow
- SBS bunker: 3+0.4? racks; Doghouses: 0.3+0.3 racks; INJ: 0.8+ rack

Counting Mode Data Acquisition and Trigger



Plan to include amplifier within the thin quartz PMT assembly; use NIM amps in US bunker if needed for others

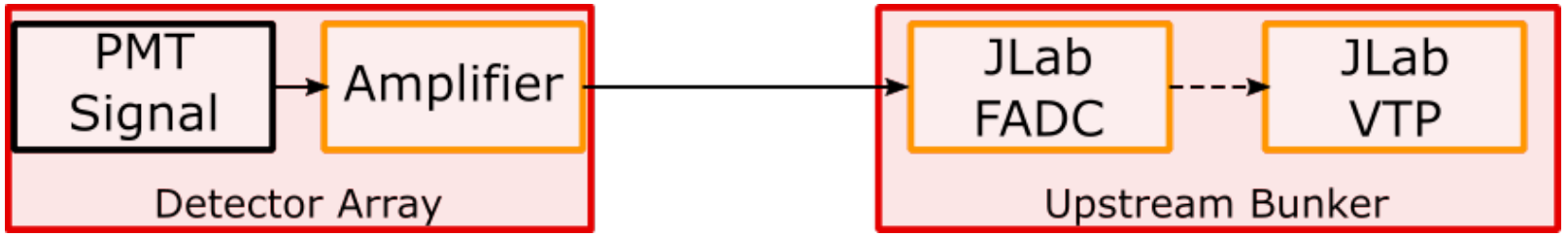
- Voltage and timing data: 320-336 ch. (20-21 FADC)
  - Detector array PMTs: 280 total; 224 thin quartz, 28 shower-max, 28 pion detectors
  - Trigger scintillators: 18; 2 each for 7 GEM sectors & 2 pion sectors
  - Scanner PMTs: 6; 2 in X/Y scanner and 1 each in 4 linear scanners
  - Alternate trigger signals: 16-32; SAM- or LAM- signals? Diffuse background PMTs? Halo PMTs?
- Voltage data only: 23 ch. (2 FADC)
  - Beamline: Two cavity triplets and two stripline BPMs: 14 ch.
  - Raster readbacks: 2 ch.
  - Scanner position: 7; 2 for X/Y, 4 for linear scanners, 1 voltage reference
- GEM readout: APV25→MPD→VTP
- We are considering if some channels may still go to a VETROC

Timing requirements for counting mode are met by the FADC250

The following are summarized from David's https://dilbert.physics.wm.edu/Tracking/36

- The charged particle flux through the scintillators will be completely dominated by the Moller and e-p electrons. Requiring both scintillators to fire will suppress the soft photon backgrounds even without a precise timing coincidence
- The APV use 25 ns bins, and the time resolution of GEMs (in SBS) is about 10 ns. The only background in the GEMs should be clusters of strips hit caused by soft photons converting in a single GEM; these could be suppressed by timing, but given the 25 ns binning of the GEM signals, an additional smearing of the trigger timing by the 4 ns binning should not degrade our ability to do this.
- Main detector and showerMax signals should be dominated by the "real" Moller + ep events. I can't see how higher resolution timing will improve our ability select hits in the quartz detectors that are true signal events.
- "Random" coincidences are actually going to be dominated by two real Moller or ep electrons in the same sector in a given time window, so improved time resolution will not allow us to significantly suppress false events from randoms.
  - FADC data should make it possible to recognize pile-up events

Conclusion: using FADC alone should be sufficient



Including amplifier within the PMT assembly is under consideration; otherwise use NIM amps in US bunker

- Trigger timing resolution of 4 ns should be sufficient, and pileup should be identifiable in the FADC. Pulse timing in analysis should be better than 4 ns.

- Removing the discriminator and VETROC allows a single cable from detector to the FADC input and simplifies the system
  - Using the VETROC would require also adding a splitter (active or passive) in the bunker

- Keeping the discriminator and VETROC would give somewhat better timing, and some redundancy. However, the key data for the quartz is amplitude, so VETROC alone insufficient.

Counting Mode Triggering

- GEMs/trigger scintillators inserted
- reduced beam current (≈100 pA) [100pA → Moller rate is ~30kHz/septant]
- use of thin ^{12}C targets, and the lH_2 target
- some measurements with "sieve" collimator to select scattering angles

1. Primary Counting-Mode Trigger
   - Trigger: "OR" of $i = 1,7$ of $[TS^i_{up} \cdot TS^i_{down}]$
2. Quartz-triggered mode
   - Triggers: possibility to select:
     a) OR of all thin quartz detectors in a given ring
     b) OR of all ShowerMax detectors
3. Pion-triggered modes
   - Triggers: possibility to select from:
     a) OR of all 7 pion detectors (cosmics, setup)
     b) OR of the two $(i = 1,2)$ ANDs: $[\pi TS^i_{up} \cdot \pi TS^i_{down}]$ (main pion dilution measurement)
     c) [OR of all 7 pion detectors] · [OR of all $TS^i_{up} \cdot TS^i_{down}$] (rate symmetry of pions; πTS efficiency; enhance pion signal)

Counting DAQ rates & data size

- FADC trigger window range: 100ns (25 samples)
- GEM samples: 3 25-ns samples

- Total Moller rate: 135 GHz@65 uA → ~300 MHz/sector/uA
  - At 100nA, ~30MHz/sector, 3 hits/sector/100ns
    - Likely use a pulser trigger at this beam current and find scint. hits in analysis
  - At 100pA, ~30kHz/sector

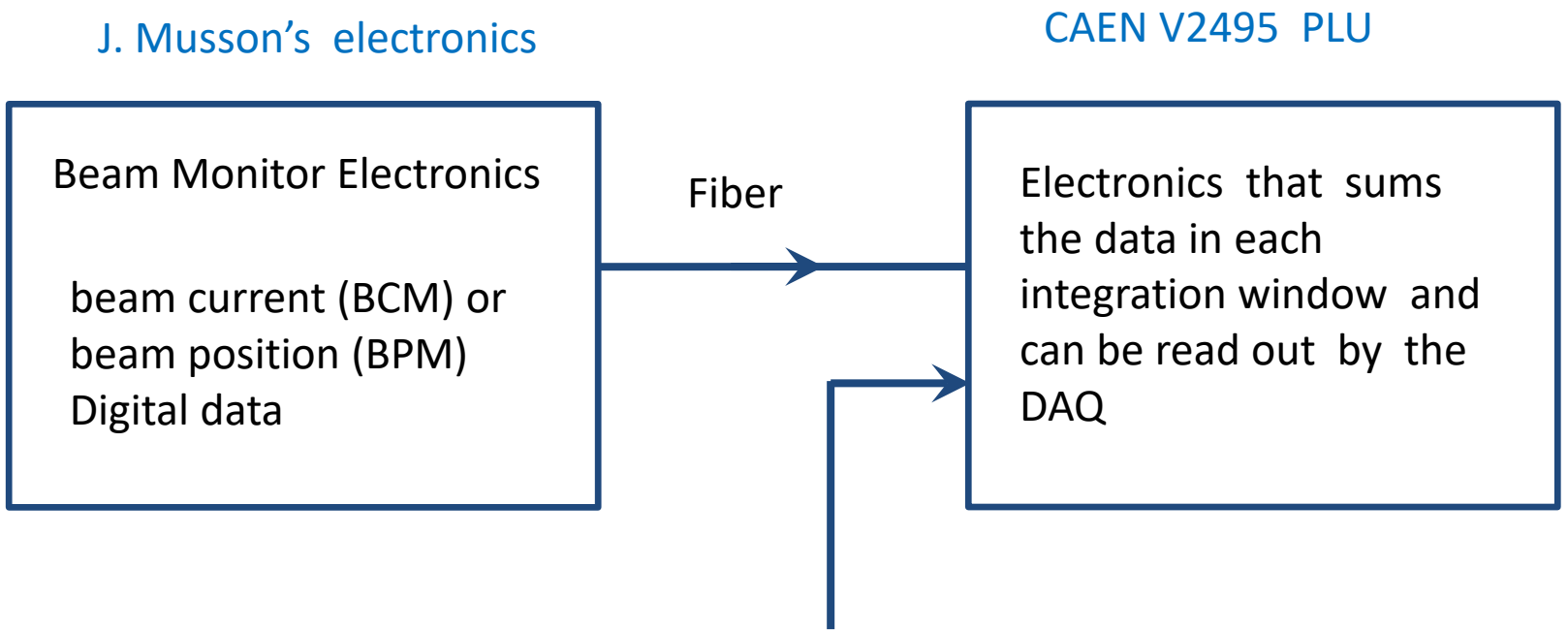
- FADC raw mode data rate at 7kHz: 150 MB/s
  - 336 FADC channels * (25 samples * 2 bytes/sample + 4 bytes for channel) → 127 MB/s
  - Estimate 8 particles with 5 detectors hit (2 scint, 1 quartz, 1 showermax, & 1 pion) in each sector per trigger; pulse parameter data would give ~23 MB/s

Beamline readout

- Expect to use Berkley digital receivers for our primary BCMs
- BPMs (and any BCMs we need to share with OPS) would (probably) go through JLab instrumentation
- Discussion group: Yury, Kent, Mark P., Bob, Jim, Paul K., John Musson
- PVES results published to date have relied on Switched Electrode Electronics for BPMs
  - With the sample and hold cards, the linac SEE effective analog bandwidth is ~30kHz.
  - SEE systems are gradually being replaced, but many likely to remain in use, such as in INJ
- New BPMs in the hall would be instrumented by JLab digital recievers
  - Normally, stripline wire-pairs are multiplexed like in SEE, but at 1 MHz switching
  - 16-bit 1 MHz analog outputs are available, with limiting bandwidth between 100-200 kHz.
  - Digital output processing would allow ~21 bits at 1 MHz sampling
  - New development work may allow removal of multiplexing and increase of sample frequency
- Digital readout system development test stand is being set up
- Plan to test new receivers in parallel with existing SEE systems on some devices

Planned Readout of Digital Data for Beam Monitors

https://userweb.jlab.org/~rom/digibcm



John Musson
Chad Seaton
Bob Michaels
Randall McClellan (initial version)

This development is supported by Hall Ops funds; would be needed for other experiments too

Slide courtesy of R. Michaels

Online Analysis

- Needed Tasks
  1. Helicity correlated (HC) feedback
     - Feedback cycle likely 10 s
  2. Monitor of data quality
     - Some issues only appear at high statistics, needing hours or days
     - Requires correction for HC beam properties
  3. Monitor of transverse beam polarization
     - Requires corrections for HC beam properties
     - Requires accumulating multiple hours of data
- Hardware needs
  - One workstation for helicity-correlated feedback
  - 10 workstations for full analysis to support #2 and #3 (~50 concurrent jobs)
  - 100 TB fileserver provides space for several days of raw data and analysis results (raw data rate is 450 GB/hr, outputs are similar in size)

Data reduction and visualization

- The total raw data volume will be at the petabyte scale
- Creating ROOT TTrees of all elements would also result in petabyte scale output files
- Several parallel data reduction choices
  - Average yields and asymmetries for all data elements over short period (~1 minute?) and store in a database
  - Generate ROOT TTrees for only the key elements for all helicity patterns
  - Keep the full ROOT TTrees for a small subset of data files
- Anticipate needing a few hundred TB of disk space to work with the output files
- We will also need robust ways to monitor system performance and present output results to analysis workers