HVMAPS Update (Compton and Ring 5)

MOLLER Collaboration Meeting
December 2021

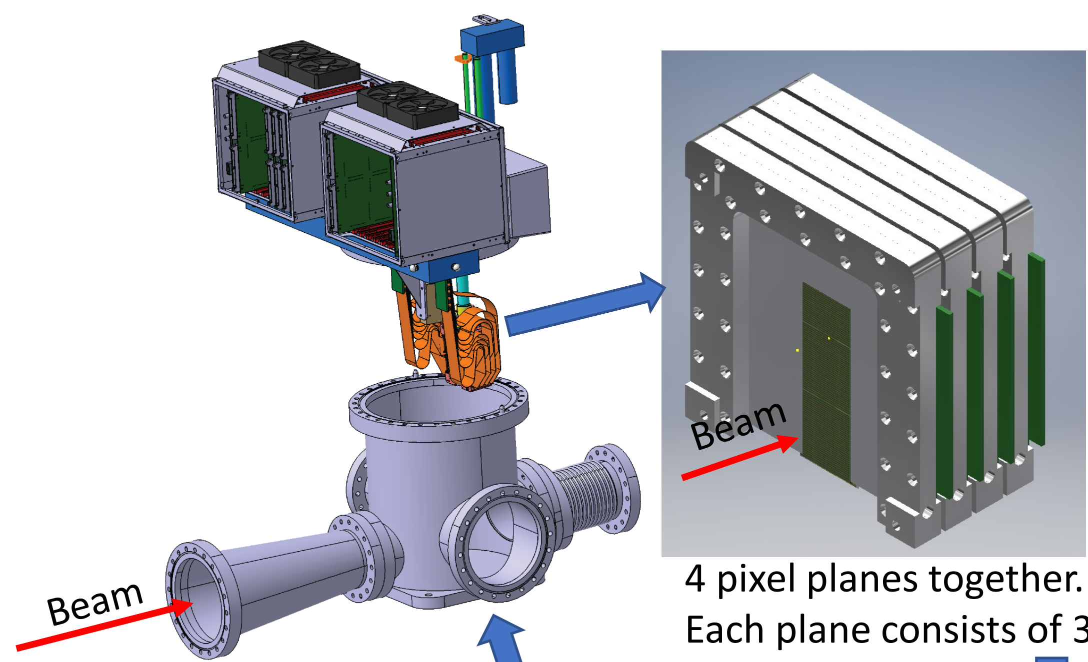
Michael Gericke

- HVMAPS for Compton
- HVMAPS for Ring 5 Profile Mapper
- General Status of things
- Near-Terms Plans

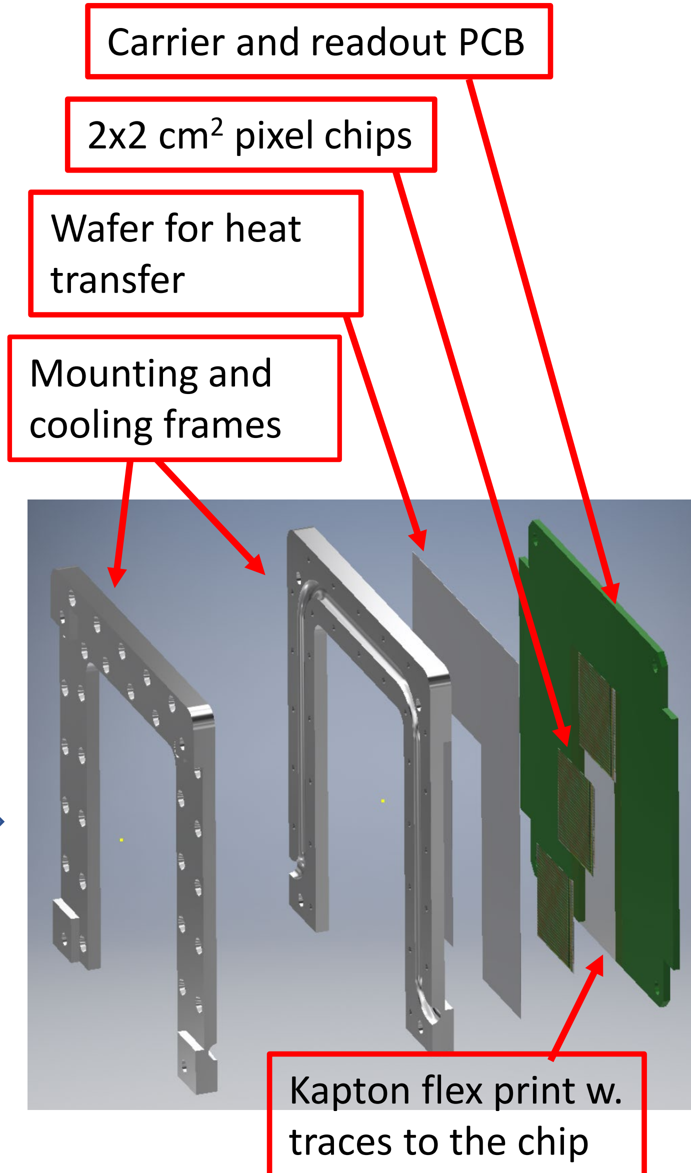
HVMAPS pixel detectors for the Compton E-Det:

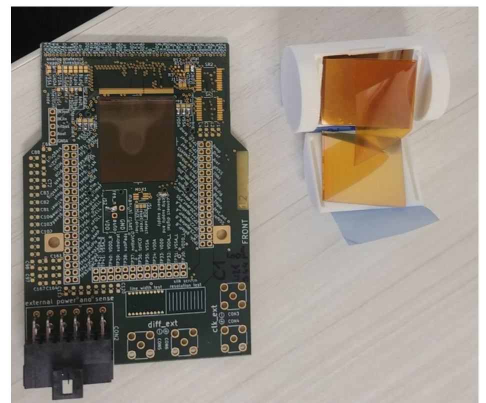
Electron detectors

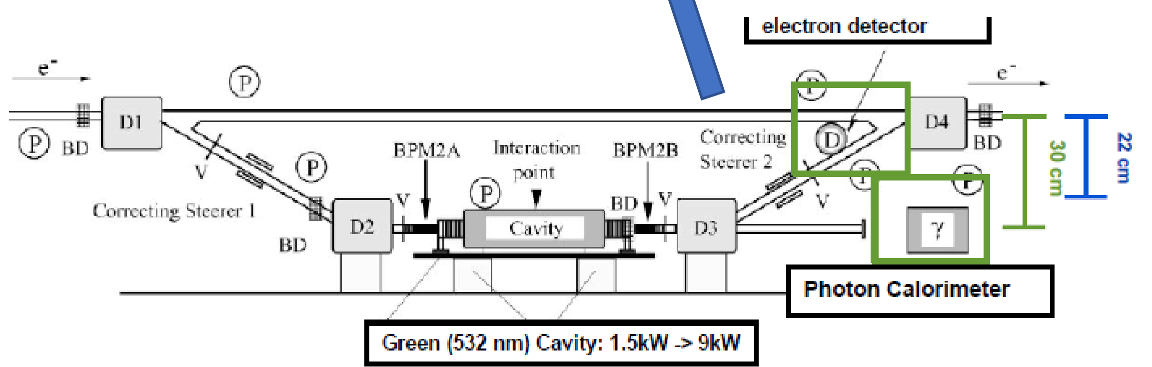
- 4 pixel detector planes
- HVMAP pixel detectors
- 3 2x2 cm^2 chips per plane
- 80x80 µm pixels



4 pixel planes together. Each plane consists of 3 HVMAP Sensors

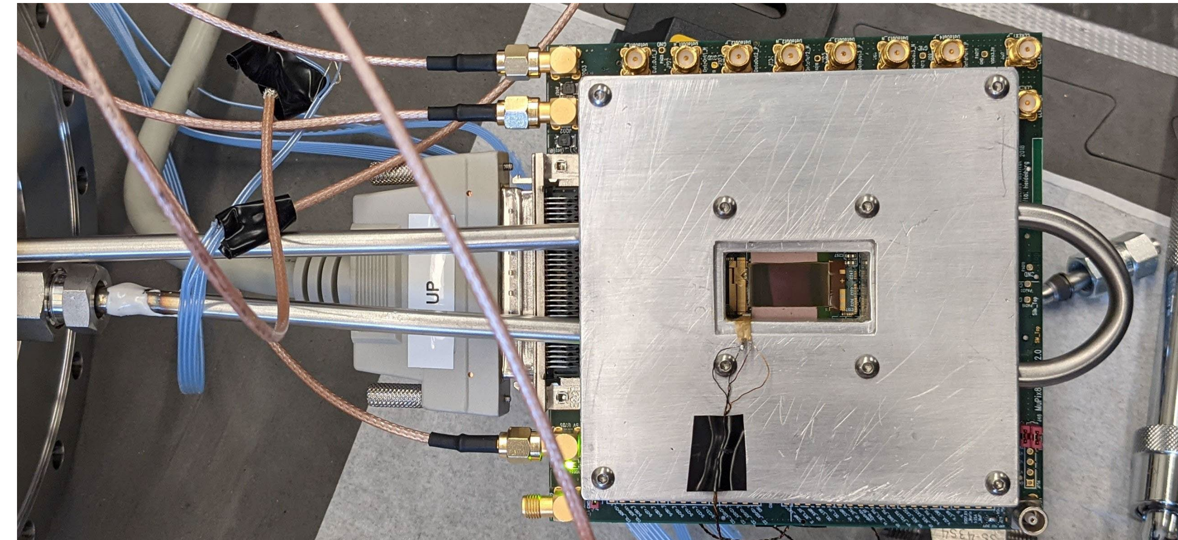




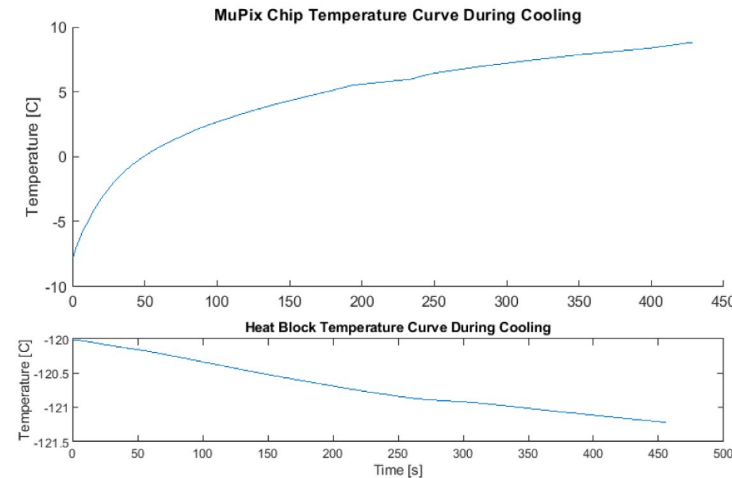


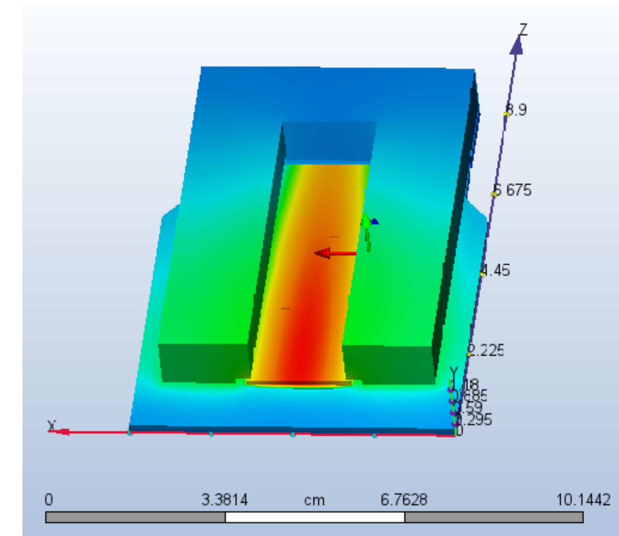
HVMAPS pixel detectors for the Compton E-Det:

- The full $2x2\ cm^2$ chip draws about 1 Watt
- We need some form of cooling inside the vacuum
- Shown on the left is a prototype board that was located in a test vacuum chamber
- Final implementation has no other electronics inside the vacuum, besides the detector chip
- The powered chip does not heat up with cooling
- Only during active readout does chip heat up
- Readout digital electronics cause draws most of the power
- Plan to have the chip edge in thermal contact with a cooled heat sink (water-glycol ?)



Work by Nafis Niloy





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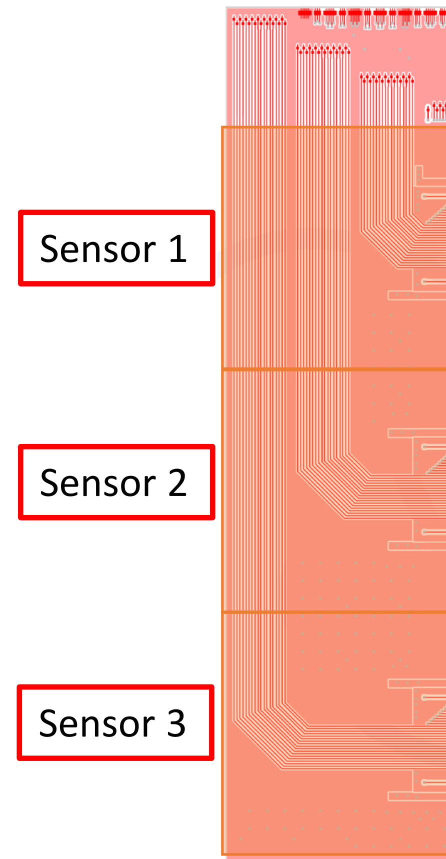
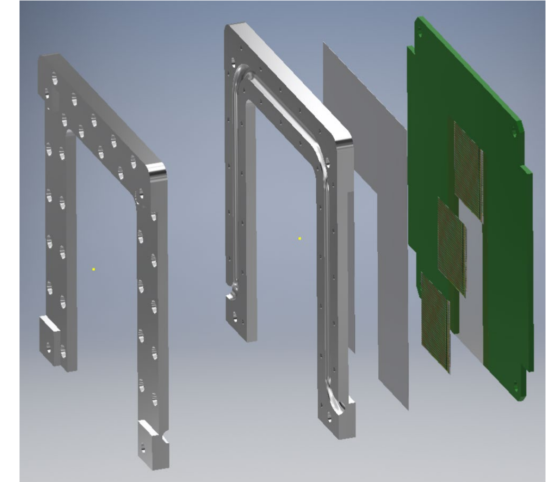
HVMAPS pixel detectors for the Compton E-Det:

- Plan to have 3 HVMAPS per flexprint
- About 30 data lines per plane + GND, VDD, Sense
- Flexprint to end of chip block PCB – then connect to ribbon cable
- Ribbon to outside vacuum onto custom designed readout board:
    - Main purpose is to connect to commercial FAPGA board
    - Considering rad hard CERN developed lpGBT and VTRX+
- Need to produce new translation stage and top-flange design
- Continue with actual mounting block design and more cooling tests this summer.
- Plan is to use final MuPix design for this purpose – delayed by a few months

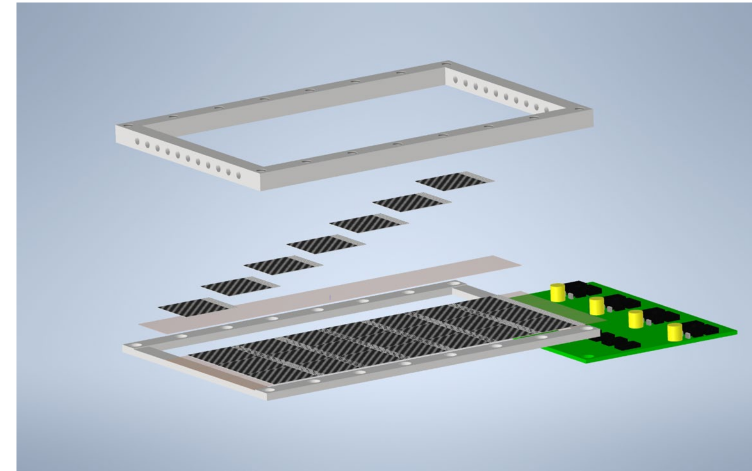


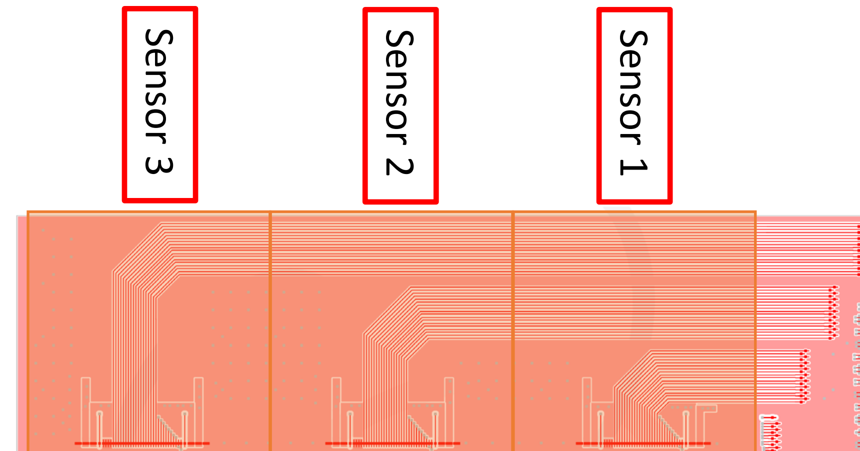


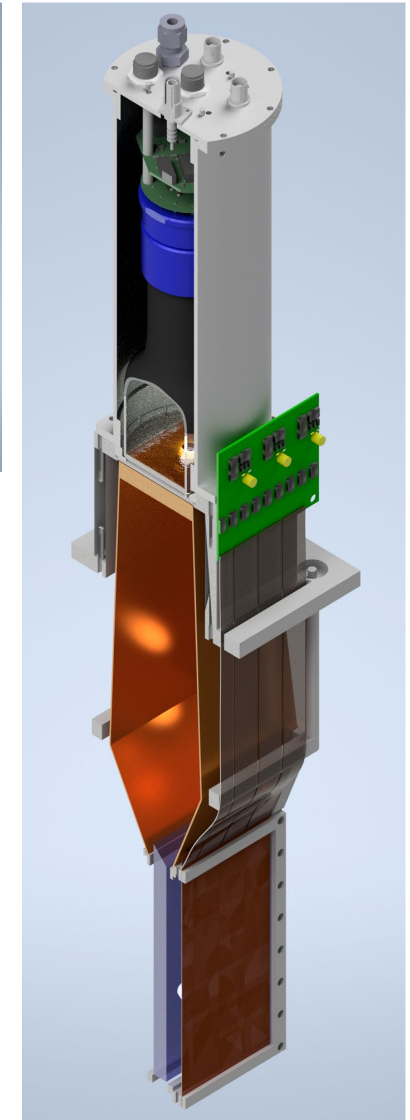
HVMAPS for ring 5 profile pixel detectors

Conceptual design for each Ring 5 Quartz tile

- bond 7 chips to a flex-print
- have 4 such strips per detector
- secure strips between the two frames
- two component $100 \times 154\ mm^2$ frame to stretch the flexprint and provide air flow
- Flexprint / ribbon cable past the light guide and through the module mount plate to readout board
- 28 chips per ring 5 tile – 28 Watt (!)
- 20 meter cable would be gauge ~13 – one for each chip + return and sense



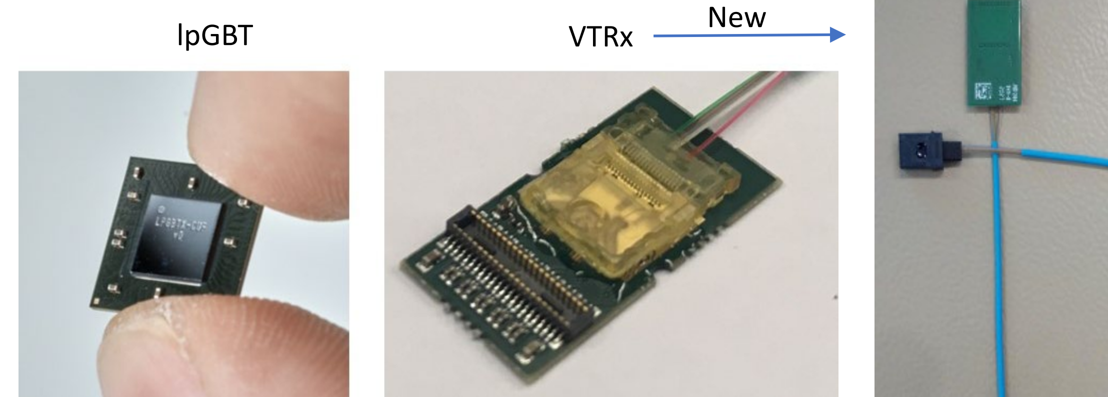




HVMAPS for ring 5 profile pixel detectors

Conceptual design for each Ring 5 Quartz tile

- Readout from the detector module can be done via low power gigabit transceiver (lpGBT) SER/DES chip and the associated VTRx optical transceiver.
- Both were developed by CERN for the LHC experiments and are radiation hard
- Verified that we can place order from CERN directly from Manitoba
- Nilanga purchased a full set for us to prototype with (thank you !!!)
- The other end would be a commercial Xilinx FPGA board – Xilinx kcu105 currently used for prototyping



New HVMAPS chip production to start in 2022:

- Implement gated readout from chip
- Adjust design to match the lpGBT protocol
- Can use one lpGBT for 7 HVMAPS
- Can use one VTRx for 4 lpGBT chips
- Readout 28 HVMAPS with this combination
- Need 84 fiber connections (VTRx)
- Need 336 of the lpGBT chips
- Readout (TX) at 1.28 Gb/s
- RX at 160 Mb/s

HVMAPS for ring 5 profile pixel detectors

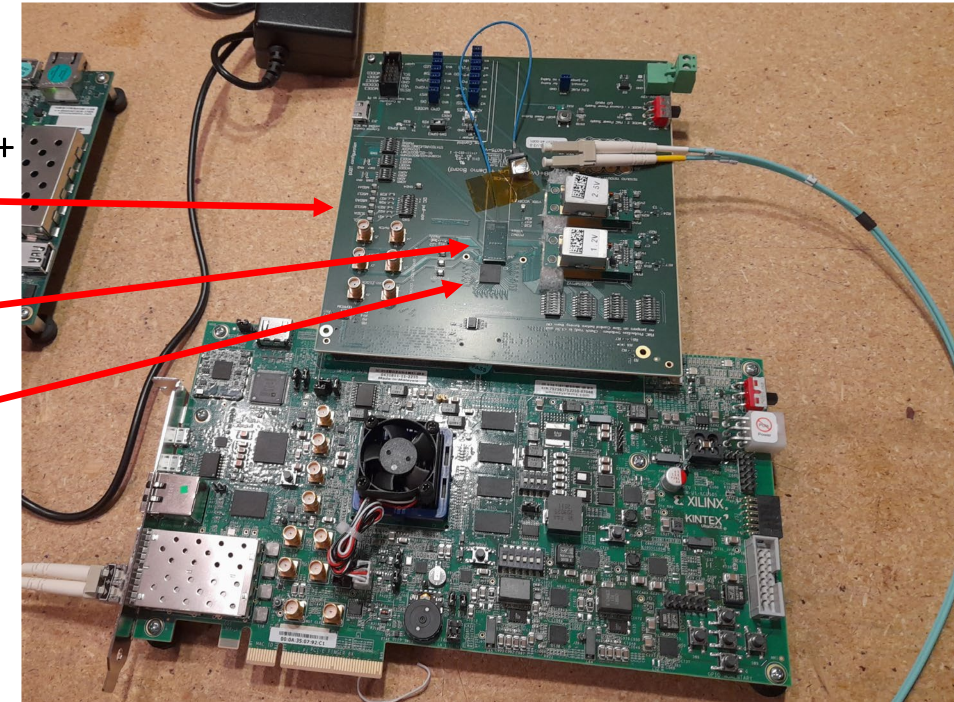
Prototyping:

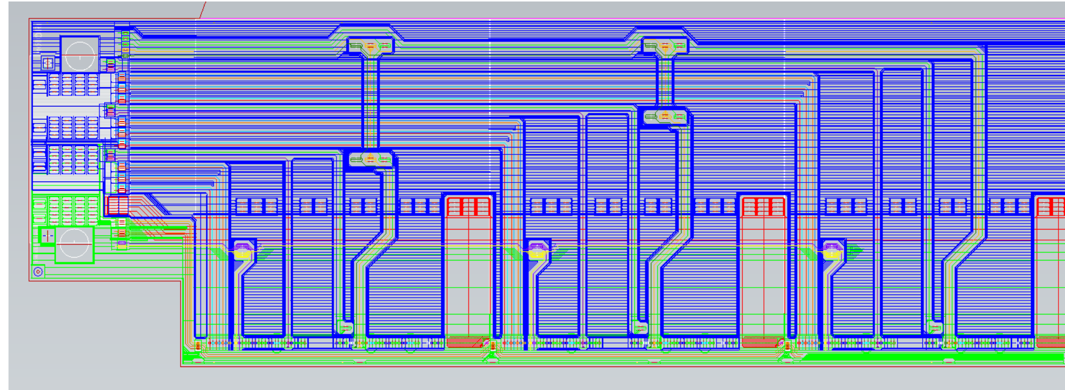
- Started to work with the CERN test board
- Both the lpGBT and the VTRX+ need to be integrated in custom readout boards
- Flexprint development underway

CERN lpGBT and VTRX+ test board

VTRX+

lpGBT



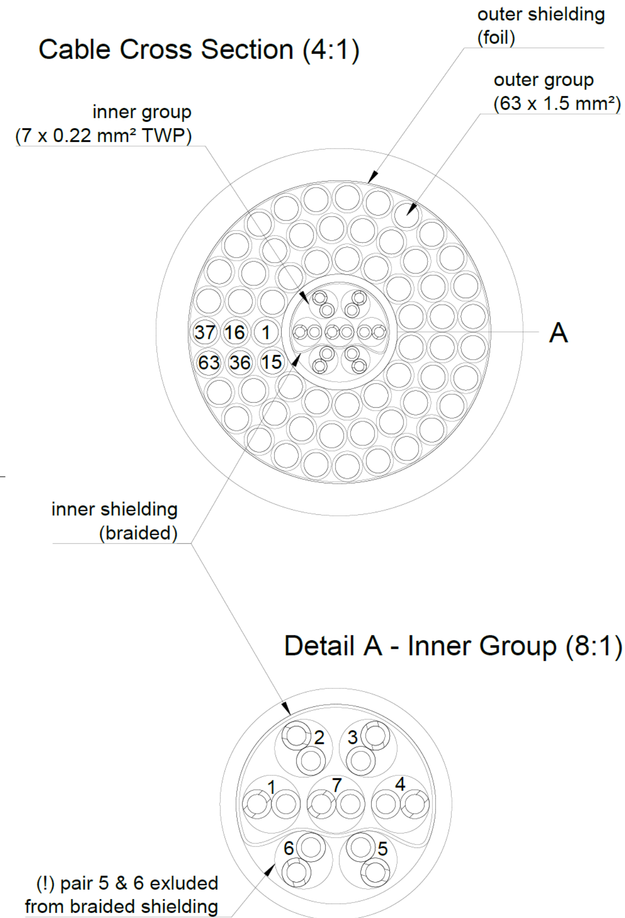


Work by Preeti Pandey

HVMAPS for ring 5 profile pixel detectors

Cabling:

- Cable design for the P2 HVMAPS tracking detector
- We would need ~2 of these per segment
- Shorter cable is definitely better …
- We would need three fiber connections per segment



Outer Group			
Conductor No.	Count x Colour	Construction	Electrical
1, 3, 5, 7, 9, 11, 13, 19, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 45, 47, 49, 51, 53, 55, 57, 59, 61	29 x RD	1.5 mm² (65 x Ø0.16)	27 A @ 2.0 V
15, 63	2 x WH	1.5 mm² (65 x Ø0.16)	2.25 A @ 1.2 V
17	1 x BL	1.5 mm² (65 x Ø0.16)	0.4 A @ 2.5 V
2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 44, 46, 48, 50, 52, 54, 56, 58, 60, 62	31 x BK	1.5 mm² (65 x Ø0.16)	29.65 A @ 0 V (RTN)

Inner Group			
Pair No.	Colour	Construction	Electrical
1	GN-WH	2 x 0.22 mm² (7 x Ø0.203)	RSEN_2V0_P (2 V nom.)
	GN		RSEN_2V0_N (RTN)
2	YE-WH	2 x 0.22 mm² (7 x Ø0.203)	RSEN_1V2_P (1.2 V nom.)
	YE		RSEN_1V2_N (RTN)
3	RD-WH	2 x 0.22 mm² (7 x Ø0.203)	RSEN_2V5_P (2.5 V nom.)
	RD		RSEN_2V5_N (RTN)
4	BK-WH	2 x 0.22 mm² (7 x Ø0.203)	RSEN_HV_P (100 V nom.)
	BK		RSEN_HV_N (RTN)
5	GY-WH	2 x 0.22 mm² (7 x Ø0.203)	10 mA @ 100 V
	GY		10 mA @ 0V (RTN)
6	PK-WH	2 x 0.22 mm² (7 x Ø0.203)	10 mA @ 100 V
	PK		10 mA @ 0V (RTN)
7	BN-WH	2 x 0.22 mm² (7 x Ø0.203)	TBD
	BN		TBD

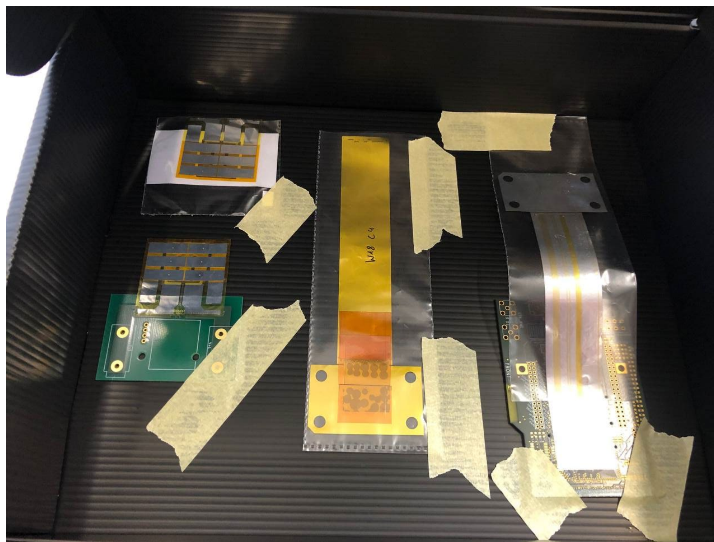
Dept.	Technical reference	Created by	Approved by
		Lars Steffen Weinstock 29.12.21	
AG Berger		Document type	Document status: PRELIMINARY
		Title: P2 Tracker Supply Cable Ver. 0	DWG No.
			Rev. / Date of issue / Sheet: 1/1

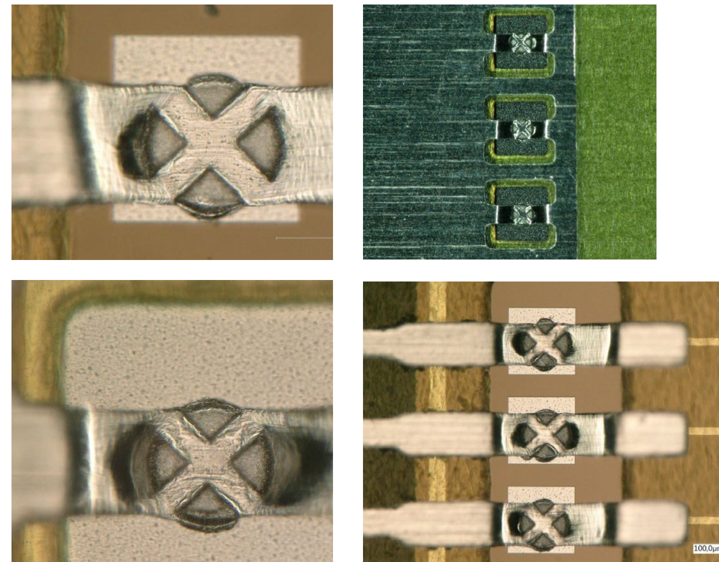
HVMAPS for ring 5 profile pixel detectors

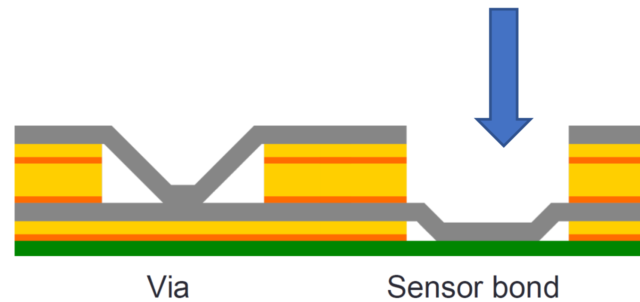
Conceptual design for each Ring 5 Quartz tile

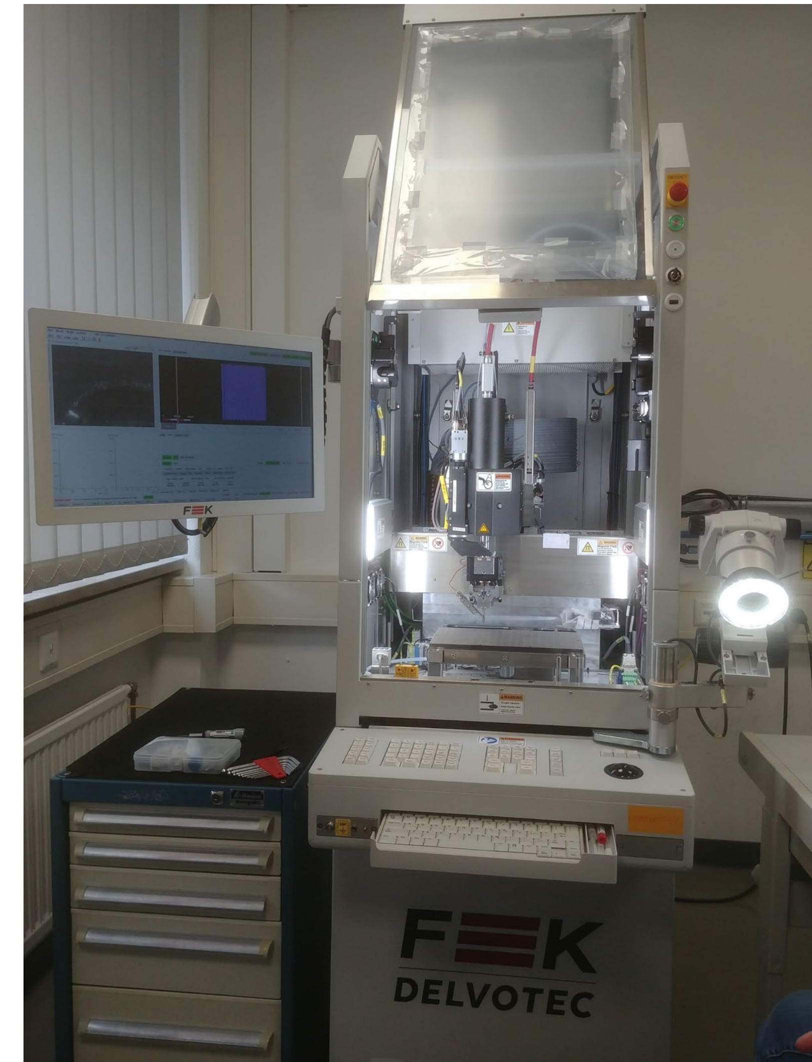
- Flexprint-chip prototype test bonding was done in October
- Purchase of bonder completed

Bonding samples









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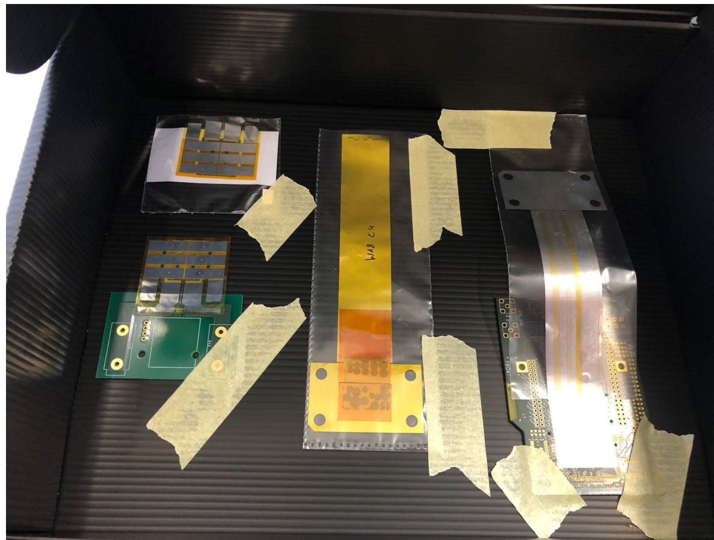

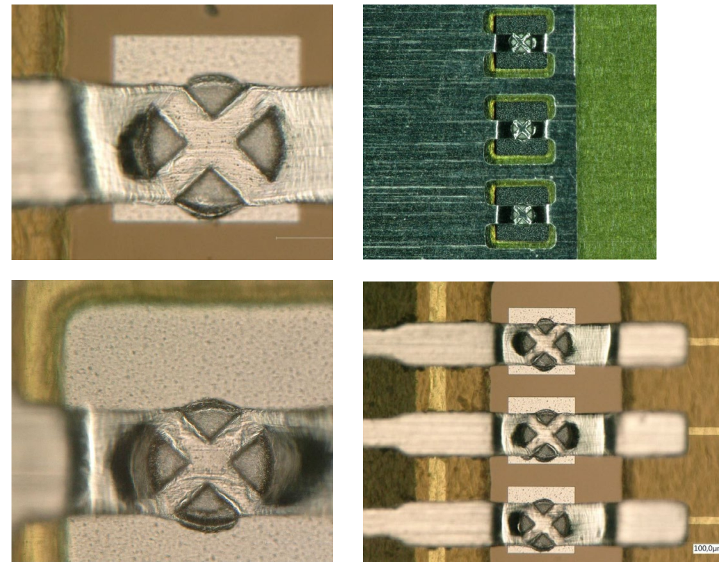

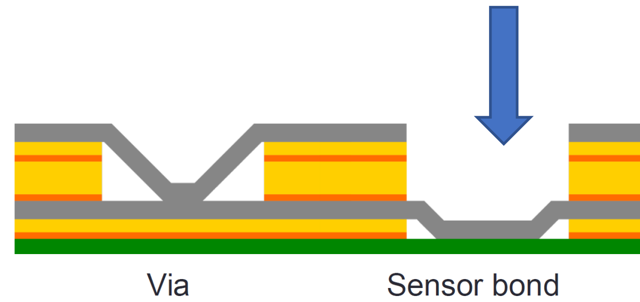

HVMAPS for ring 5 profile pixel detectors

Near-term tasks:

- Complete flexprint design for both, the 3 chip Compton ladder and the 7 chip ring 5 ladder (issue: Flexprint company is located in the Ukraine)
- Modify chip design to include gating option and match to lpGBT clock (depends on designer schedule)
- Develop prototype mounting structure for Compton E-det and redo cooling tests (Nafis)
- Develop prototype readout board (issue: Recently lost engineer to industry – rehiring)
- Develop mounting structure for ring 5 profile mapper and cooling concept
- Develop gluing and bonding setup for the HVMAPS flexprint assembly (Nafis)

The biggest issue at the moment is lack of people working on the HVMAPS.