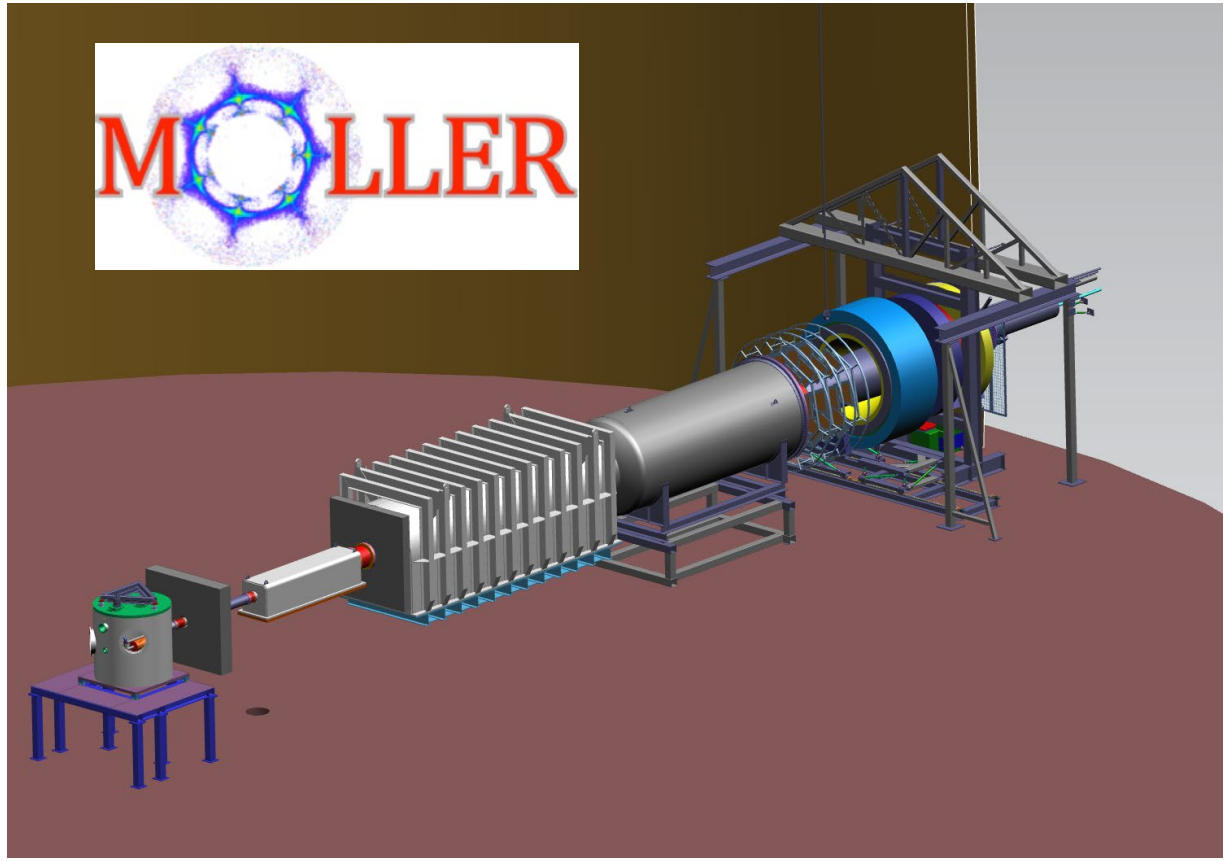
DAQ update

Integration and counting mode DAQ planning for MOLLER (WBS 1.07, 2.07, 3.07)

MOLLER Collaboration meeting, 21-22 June 2022



OHIO UNIVERSITY

Paul M. King – Ohio University

MIE WBS1.07 Level 2 Technical Lead

Jefferson Lab

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Milestones & Plans (As of Dec. Collab. Meeting with updates)

- Verification of test system: Oct/Nov 2021 – Feb/Apr 2022
  - ~~Ohio just received the VXS crates and VME CPUs; ADC modules will be available later (Feb? March?) May push the test system verification into May?~~
  - Integrating ADC now expected to be at JLab ~July; testing to go into August-September?
- 90% design preparation and review: Apr 2022 – May 2022
  - ~~Trigger and DAQ FDR is proposed for June 9-10~~
  - Now anticipate Trigger and DAQ FDR at end of summer (not yet scheduled)
- Support of PQB studies
  - Currently only using INJ crate with VQWKs, running CODA 2.6.2
  - GEn-II will be running a counting house parity DAQ for charge feedback; may allow PQB studies through to the hall
- For the 90% review (or sooner), need to have the plan for certifying the electronics modules with the new guidance from Electrical Safety committee

Other things to think about before 90% review (As of Dec. Collab. Meeting)

- Helicity readout options
  - "Traditional" helicity readout using IO registers & scalers with some NIM signal handling
  - A new helicity decoder board has been developed; a prototype is available but testing hasn't started yet
- Scalers
  - Several scalers are in the budget, but we haven't enumerated the signals we are inputting
  - If we want to scale PMT-like signals, would also need discriminators
  - Note that the FADCs have a mode in which they can provide counters of the pulses above threshold, so signals in FADCs could do without a scaler
- Beam modulation
  - The beam modulation system itself is hall infrastructure
  - Modulation cycle start should be synchronized with DAQ; details may depend on modulation frequency, etc
- What else?
  - Do any subsystems need slow controls/EPICS support that they haven't already included?

Developments since December 2021

- Continued development of integrating ADC
- New polarimeter DAQ being developed in TEDF test stand; very similar to counting DAQ design
- Planning for beamline readout
- Discussion of new helicity generator patterns
- Restart of mock-data development within japan; analysis group should start meeting “soon”

Integrating ADC update

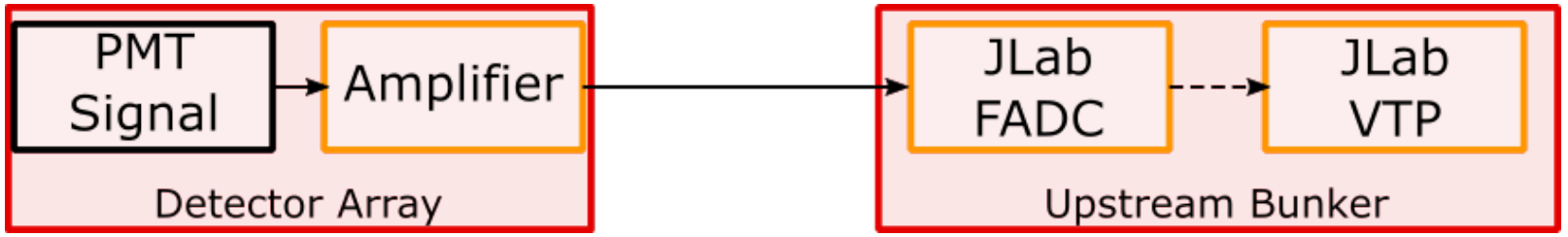
- We have five 16-ch prototypes of the ADC module
  - Two amplifiers in the input stage need to be changed; parts expected at beginning of August
  - With the currently installed amplifiers, the gain is 100x lower than planned.
- One 16-ch prototype had the input stage modified and was used for Mainz test beam; worked well
- Prototype uses Power over Ethernet (PoE++); considering this for the experiment instead of having separate power supplies
- Expect to ship an unmodified prototype to JLab this week to begin CODA development
  - When the amplifiers arrive, JLab FEG will replace them instead of shipping back to TRIUMF
- Beginning discussions about getting Electrical Safety review of the modules
  - If using PoE, the board ought to be a Class 1 electrical device, simplifying the device registration process

Integration mode channels

- Detector array (280 total)
  - 224 Main detectors, 28 shower-max detectors, 28 pion detectors
- SAMs, LAMs, and beamline (233 channels)
  - SAMs: 8
  - LAMs and diffuse background monitors: 28 (14 LAM + 14 DBM)
  - Injector beamline: 96
  - Transport line and Hall beamline: 87 (PREX/CREX used 64; my count so far ~77 ch.)
    - Channels needed for beamline may be lower due to LBNL & JLab digital recievers
- Scanner (6+7 channels)
  - X/Y scanner: 2 PMTs + 2 position voltages (positions might go into a FADC or VQWK?)
  - Linear scanners: 4 PMTs + 4 position voltages
  - Reference voltage for positions
- Total: 512 channels → 32 16-channel modules (increase to 34, or reduce beam chan?)

- HVMAPS & Digital BCM expect to connect into CODA in same way as ADCs

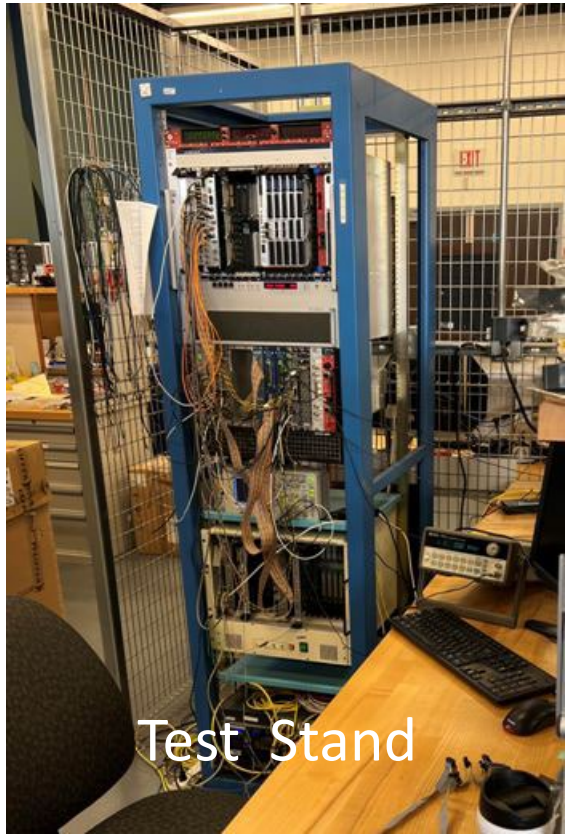
Counting Mode Data Acquisition and Trigger



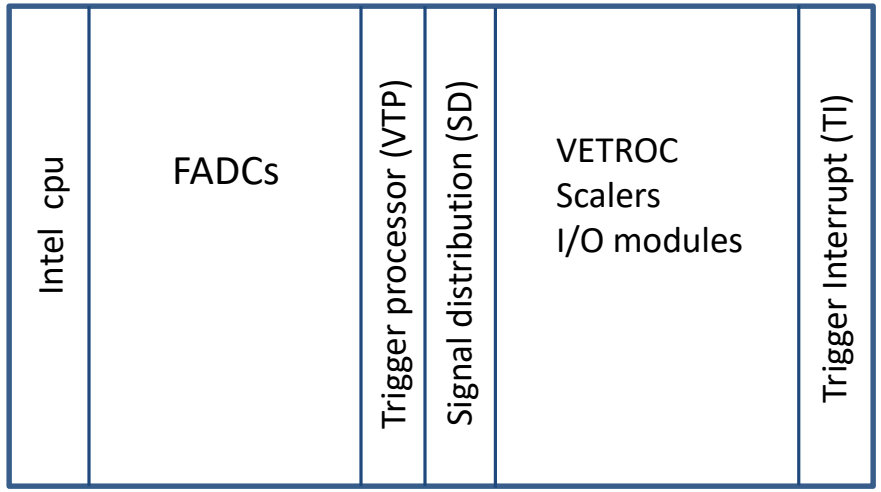
Plan to include amplifier within the thin quartz PMT assembly; use NIM amps in US bunker if needed for others

- Voltage and timing data: 320-336 ch. (20-21 FADC)
  - Detector array PMTs: 280 total; 224 thin quartz, 28 shower-max, 28 pion detectors
  - Trigger scintillators: 18; 2 each for 7 GEM sectors & 2 pion sectors
  - Scanner PMTs: 6; 2 in X/Y scanner and 1 each in 4 linear scanners
  - Alternate trigger signals: 16-32; SAM- or LAM- signals? Diffuse background PMTs? Halo PMTs?
- Voltage data only: 23 ch. (2 FADC)
  - Beamline: Two cavity triplets and two stripline BPMs: 14 ch.
  - Raster readbacks: 2 ch.
  - Scanner position: 7; 2 for X/Y, 4 for linear scanners, 1 voltage reference
- GEM readout: APV25→MPD→VTP
- We are considering if some channels may still go to a VETROC

R&D on Polarimeter DAQ for moller and compton in halls A and C



Plan: Firmware design to support both counting mode and integrating ("accumulators")



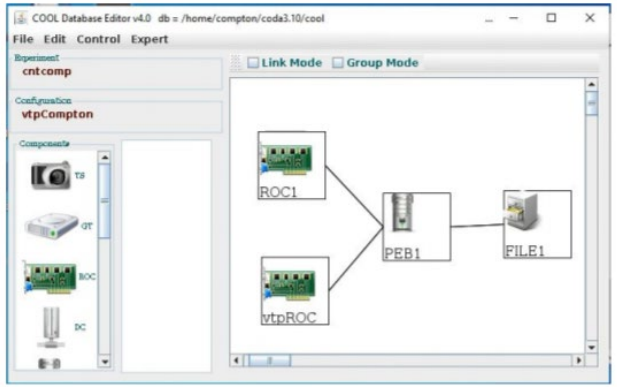
Slide courtesy of R. Michaels

Initial version of the new polarimeter DAQ ran during (P)CREX

Bryan Moffit, Ben Raydo, Alexandre Camsonne, Iris Halilovic, Bob Michaels

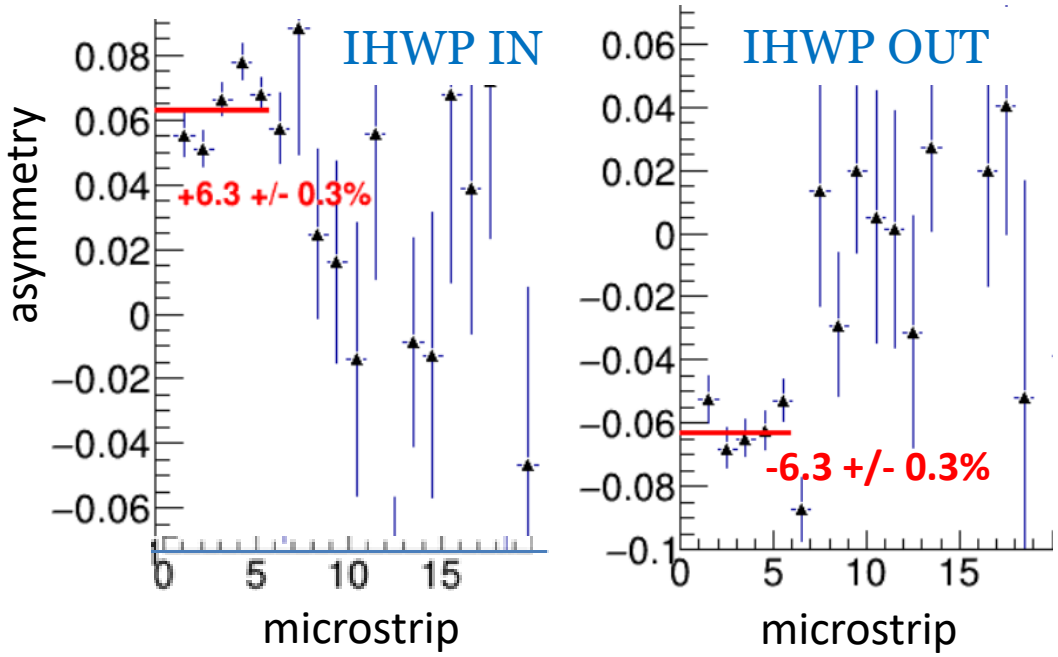
That DAQ read out the microstrips (electron detector) and phototube signals (photon detector). It used a VETROC, VTP, FADC, and scalers.

CODA configuration



Results

Asymmetries observed in electron detector.



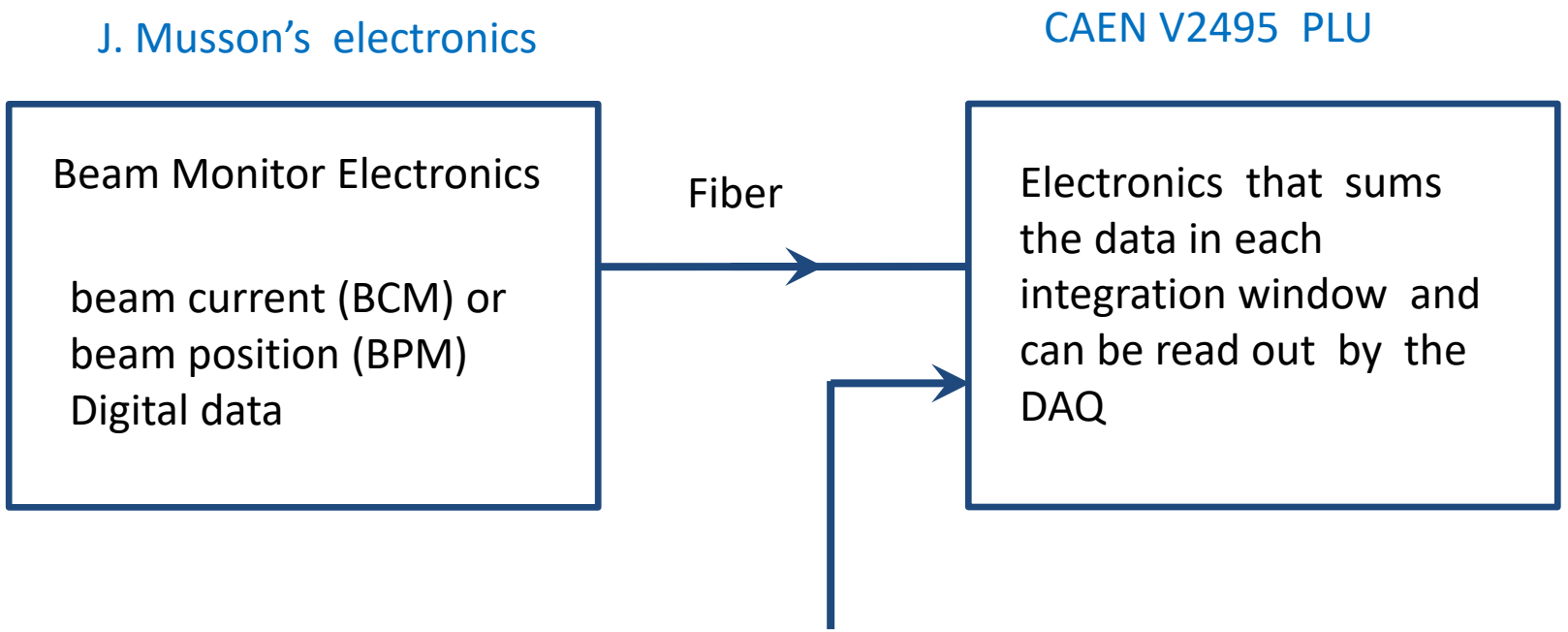
Slide courtesy of R. Michaels

Beamline readout

- Expect to use Berkley digital receivers for our primary BCMs
- BPMs (and any BCMs we need to share with OPS) would (probably) go through JLab instrumentation
- Discussion group: Yury, Kent, Mark P., Bob, Jim, Paul K., John Musson
- PVES results published to date have relied on Switched Electrode Electronics for BPMs
  - With the sample and hold cards, the linac SEE effective analog bandwidth is ~30kHz.
  - SEE systems are gradually being replaced, but many likely to remain in use, such as in INJ
- New BPMs in the hall would be instrumented by JLab digital recievers
  - Normally, stripline wire-pairs are multiplexed like in SEE, but at 1 MHz switching
  - 16-bit 1 MHz analog outputs are available, with limiting bandwidth between 100-200 kHz.
  - Digital output processing would allow ~21 bits at 1 MHz sampling
  - New development work may allow removal of multiplexing and increase of sample frequency
- Digital readout system development test stand is being set up
- Plan to test new receivers in parallel with existing SEE systems on some devices

Planned Readout of Digital Data for Beam Monitors

https://userweb.jlab.org/~rom/digibcm



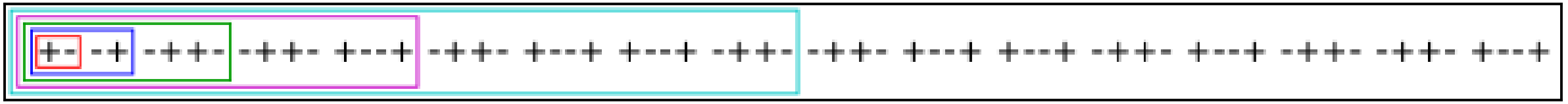
John Musson
Chad Seaton
Bob Michaels
Randall McClellan (initial version)

This development is supported by Hall Ops funds; would be needed for other experiments too

Slide courtesy of R. Michaels

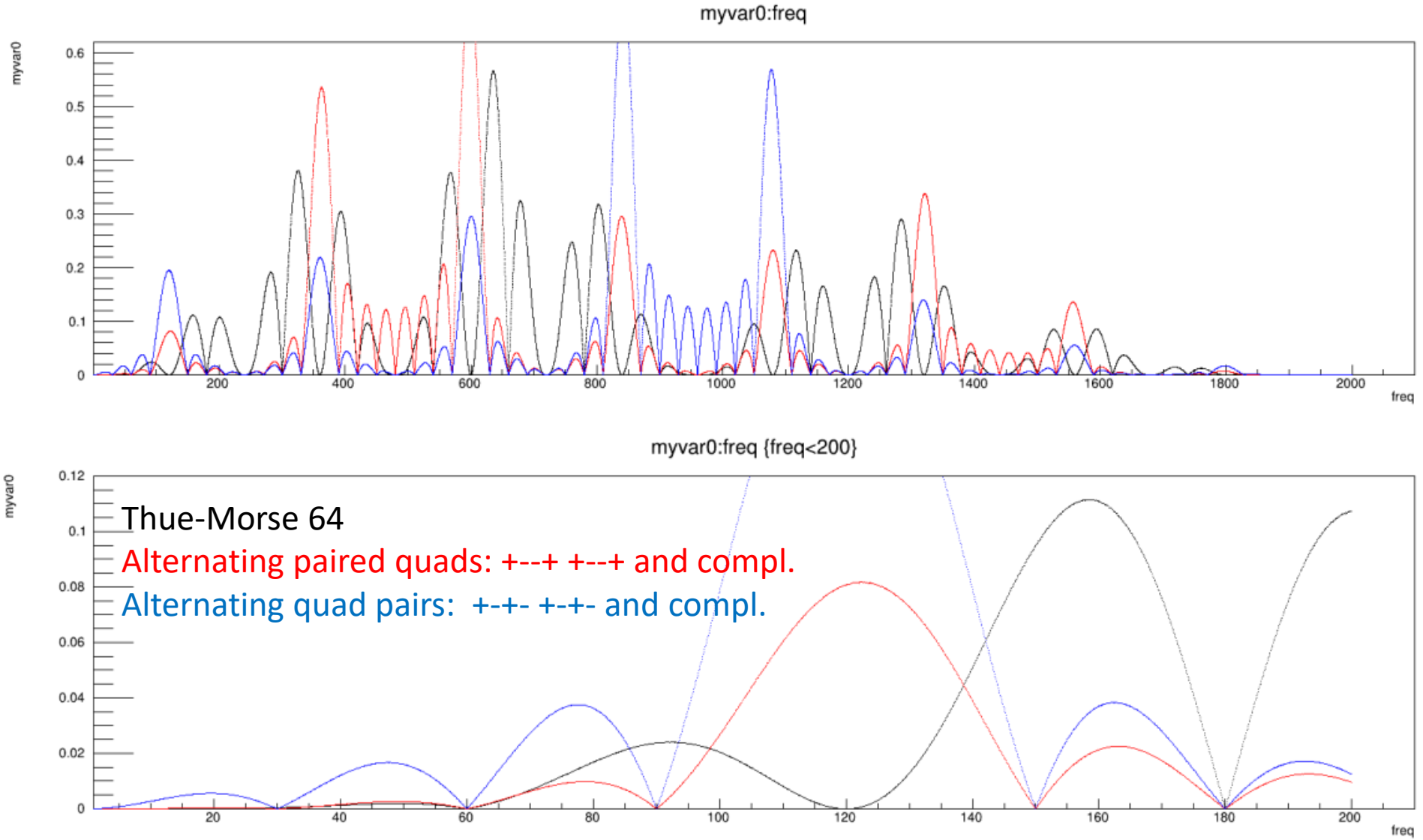
Helicity generator boards and helicity pattern

- New helicity boards being constructed (identical to current design) with new firmware
  - 1920 Hz running: 520.85 μs period, such as 510.85 μs T_stable & 10 μs T_settle
  - 64-event helicity pattern length with 128 event delay
- Discussion group for helicity pattern: Kent, Caryn, Riad, Paul K., Prasanna N.
- Plan to have three options for 64-event pattern structure: Thue-Morse; alternation of quad polarities; sequence of pairs. These could be changed in firmware if desired.
- 64-event Thue-Morse pattern: each doubling of the pattern adds inverse of previous



- Numerical integration of sine & cosine waves over 500 consecutive patterns was performed as a function of frequency, collecting the RMS of pattern differences to evaluate noise sensitivity

Modeled fractional pickup of several helicity patterns



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Mock-data and analysis testing

- Mock-data generator within “japan” creates realistic data files with time-dependent and randomized generation of beam parameters and detector signals, including correlations
- First model of the integrating ADC data-structure has been added; should be updated as we become familiar with the actual data stream
- Analysis of these data files allows testing of throughput and processing algorithms
  - Processing time for initial mock-data (216 PMT channels and 50 beamline channels) is ~5μs per event; this is faster than we had expected from scaling arguments
- We should restart the parity analysis group discussions
  - Starting point is the japan framework as used in PREX/CREX; should revisit what worked well and what was missing
  - Are there reasons to make major framework changes, or even start with new framework?
- Should also be considering the tracking analysis; should look at what can be used from SBS

Paul King

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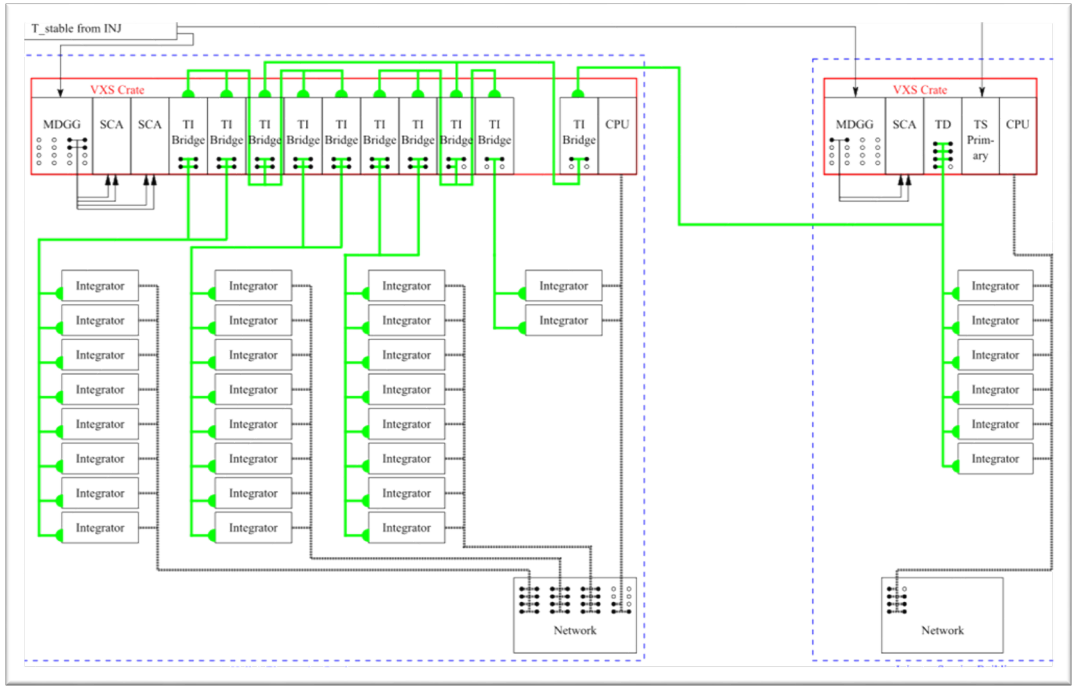
Summary

- Integrating and counting DAQ working groups are continuing to refine the designs and prepare the design and interface documents
- CODA development for integrating ADC to begin shortly
- Plan to start bench testing of JLab digital beam readout soon
- Aim for 90% design review at end of summer



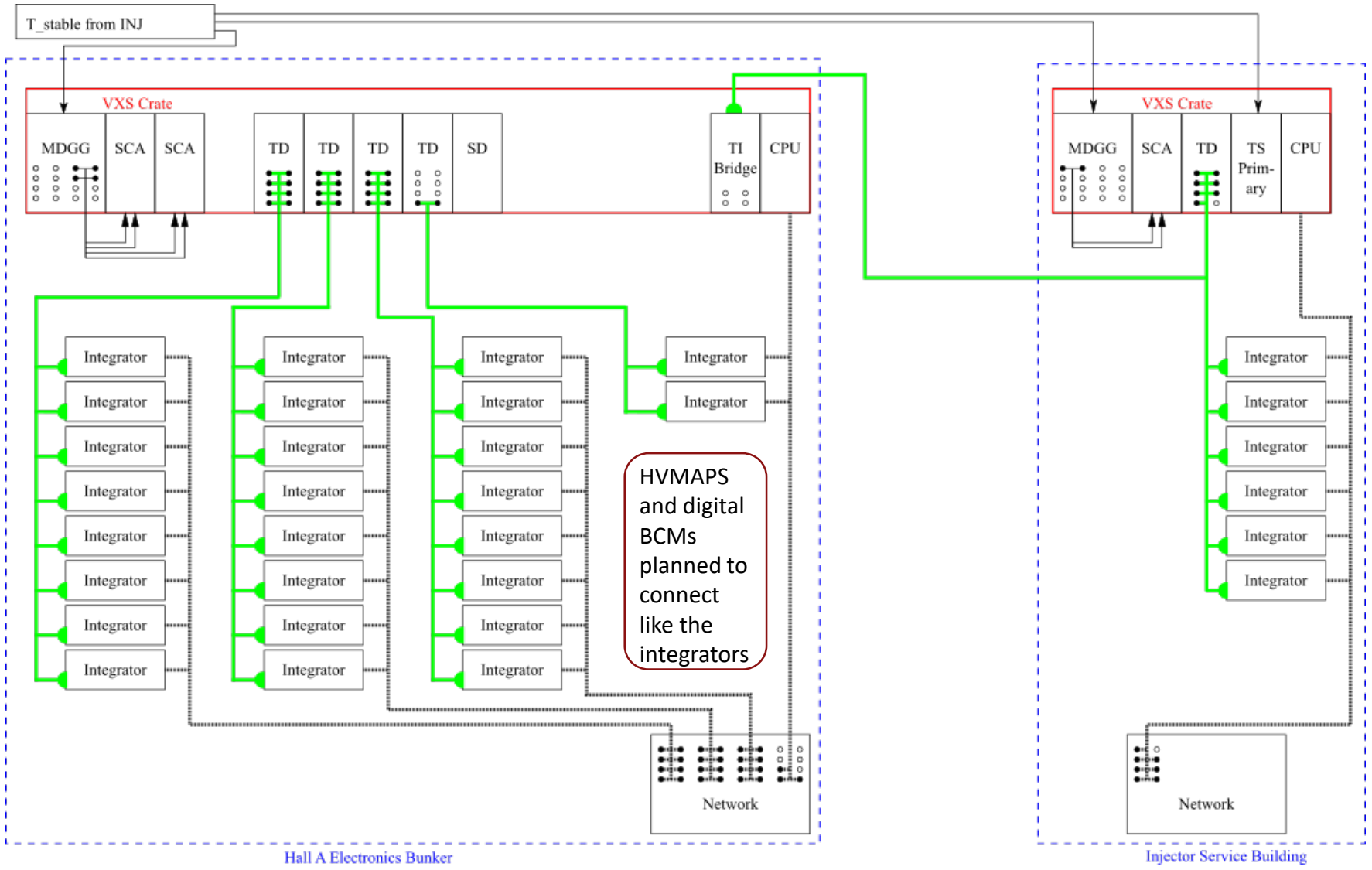
DAQ development contributors

- Integration mode
  - D. Bishop, B. Shaw; TRIUMF
  - B. Blaikie, M. Gericke, J. Pan; University of Manitoba
  - C. Cuevas, W. Gu; JLab
- Counting mode
  - D. Armstrong; William and Mary
  - C. Ghosh, H. Liu; University of Massachusetts, Amherst
- Digital BCM
  - J. Arrington, Y. Kolomensky, S. Li, Y. Mei, E. Sichtermann; LBNL
  - W. Gu; JLab

- All three teams involve
  - R. Michaels, B. Moffit; JLab
  - P. King; Ohio University

BACKUP SLIDES

Integration DAQ layout



Helicity trigger is formed in ISB, so that INJ gate is formed promptly

Gate timing adjusted per module to account for ~20µs electron transit or other signal latencies; need ~0.1µs resolution

TI Bridge feeds SD/TDs to distribute gates/triggers

TI to Integrator connection use one QSFP connection

10Gb/s network on QSFP connections

Integration ADC readout modes

- Primary mode
  - Samples are accumulated into 4 “subblocks” in each helicity window, as well as the full window accumulation
  - Each subblock has the full window has: sum, sum of squares, minimum, maximum, and number of collected samples

- Diagnostic modes are still being discussed. Some of the ideas we’ve mentioned.
  1. Streaming of all samples for a small number of channels for continuous ~1 second
     - Purpose: to carry out FFT analysis over the range of Hz to MHz
  2. Reporting of all samples in a window; there may be deadtime, with windows non-consecutive
     - Purpose: used with pulse mode beam to compare signal latency between different detector/monitor elements, and to adjust the gate timing
  3. Reporting of all samples for two or more consecutive windows; could be the same as #2 with a “special definition” of the window start
     - Purpose: used to look at behavior of signals during the “settle” period

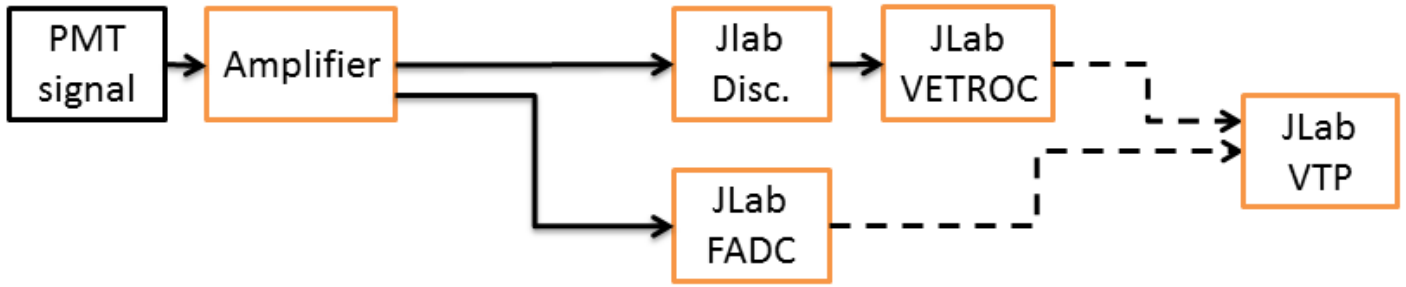
Signal levels in integration mode

- The integrating ADC module base design uses a differential input with both pins accepting a -2V to +2V range, allowing a -4V to +4V signal range

- PMT signals: the transimpedence preamplifiers are designed to match the ADC input.

- Beam monitor signals from JLab instrumentation are available as single-ended signals. Alternate front-end panel for the ADC will take single-ended input on BNC with signal range of -4V to +4V.
  - Stripline BPMs: The S&H cards output a nominal 3V signal (potentially chosen in either polarity), but the signal can go to 5V. Plan to add in-line attenuators
  - BCMs: CREX saw nominal signal levels of ~1.3V from the analog BCM receivers
  - Cavity BPMs: CREX saw <2V on the Q signals and a range of +/-1V on the position signals
  - Raster pickoff: CREX saw triangle wave with <2V amplitude; the raster is being reworked & currents will be higher → Plan to add in-line attenuators

Why don't we have the TDCs/VETROCs anymore?



In the counting mode DAQ in the CDR, we had discriminators and VETROC modules for timing. However, we think the FADC will give us sufficient timing resolution.

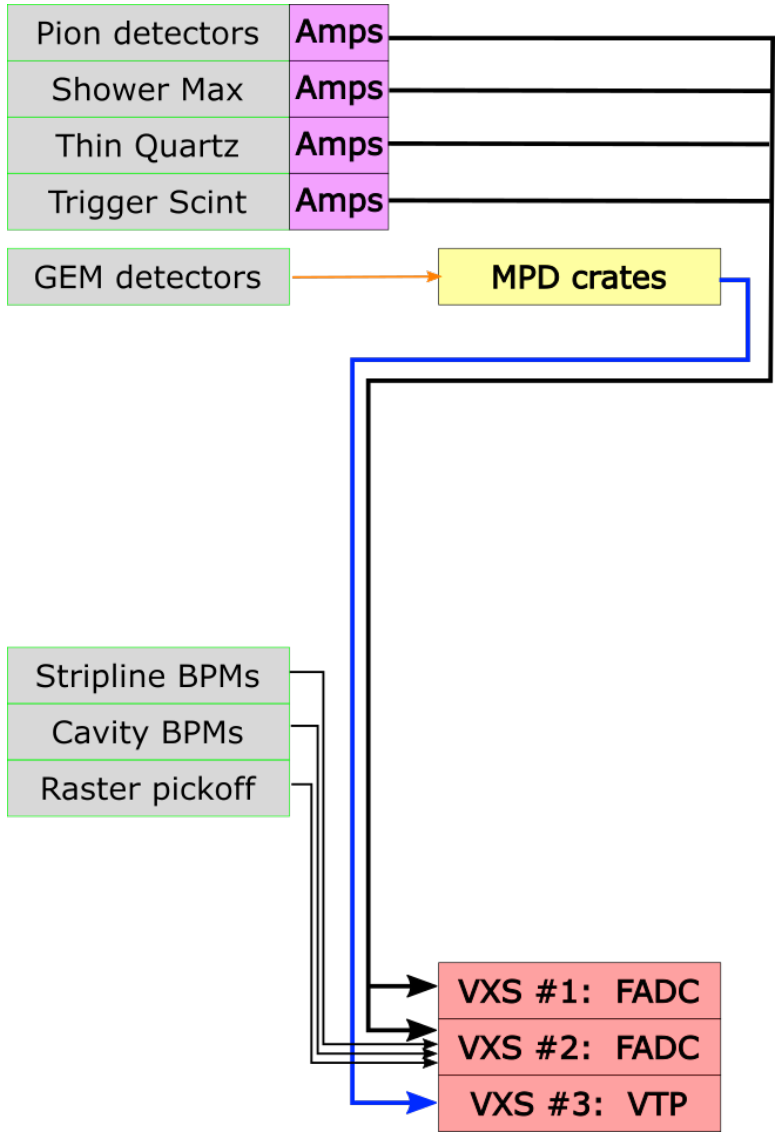
We need the timing to find coincidences between the scintillators, match to the quartz and GEMs, and have some gauge of accidentals

- FADC250 waveform has 4ns time steps
  - Fitting a peak in the waveform can get better precision; some report as low as ~60ps
  - Considering only the 4 ns bins, a rough calculation gives accidental rate of 5% of coincidences at 100 nA (Moller rate ~30MHz/sector), so can likely do better by peak fitting

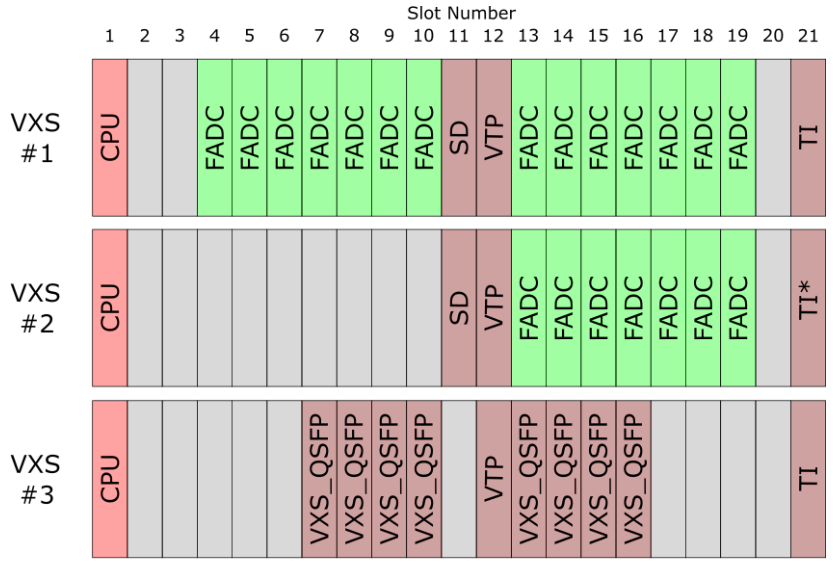
A more complete evaluation of the timing requirements is in progress.

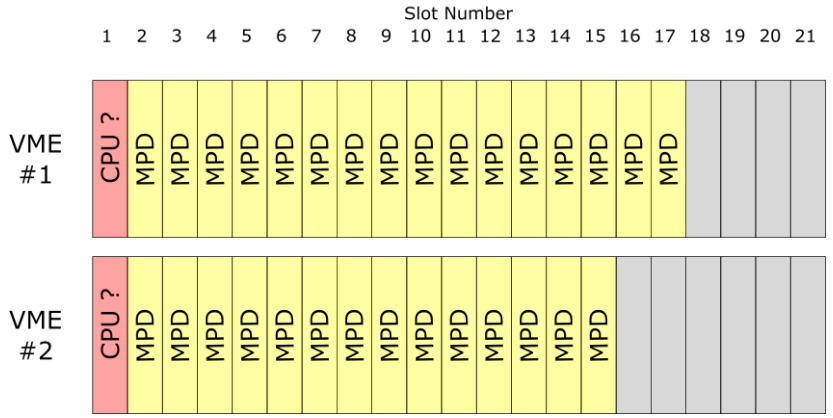
Counting mode cable and crate layout

- PMT signals go through event-mode amplifiers built into the base, then through high density cables to a patch panel, then 320’ RG58 cables to main electronics hut patch panel
- From main electronics hut patch panel, 600” RG58 cables connect to the FADCs
- Beam monitor signals run on RG58 cables (length TBD) from the standard Hall A electronics racks to FADCs
- GEM signals from 30 modules (28 tracking, 2 pion) go to the 30 MPDs in their doghouses, then to a VTP in the main electronics hut



Counting mode crate layout





- VXS #1: Rings 1 – 4, Ring 5 & 6
- VXS #2: Shower max, Pion detectors, Trigger scintillators, Scanner, Alternates; Voltage-only signals

- VXS #3: 30 MPDs readout through VTP
  - Crates of 16 or 14 MPDs in two doghouses

Trigger formation

- Trigger thresholds defined in FADCs
- FADC trigger information sent to VTP for processing
- VTPs in VXS #1 & #2 send triggers to TI-master

FADC readout may be done through VTP or VME

Signal levels in counting mode

- The FADC can have a negative going range of 0V to -2V (or similar for positive) A DAC offset allows software adjustment of the baseline.

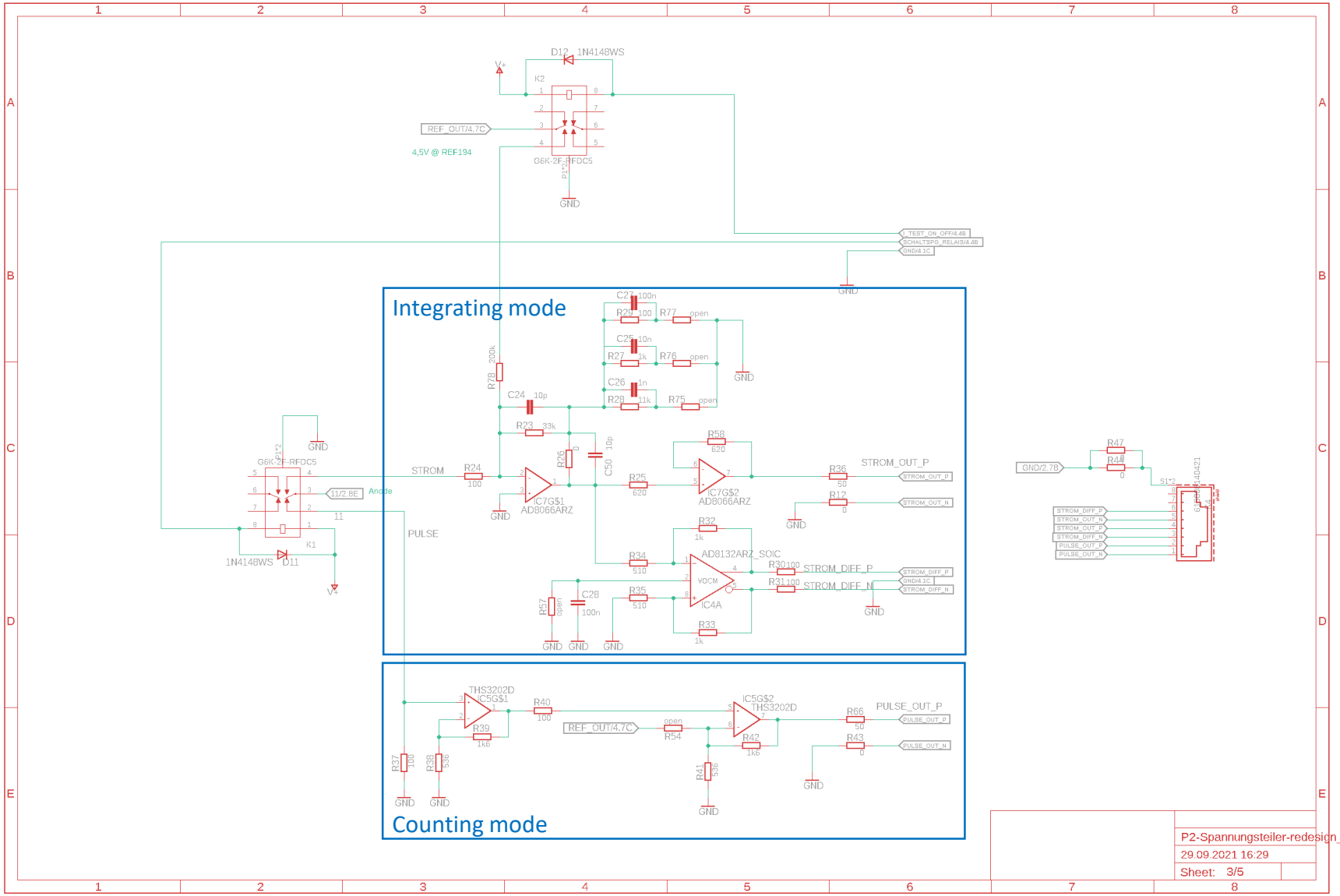
- PMT signals: Signals should be within the input range

- Beam monitors
  - Stripline BPMs: The S&H cards output a nominal 3V signal (potentially chosen in either polarity), but the signal can go to 5V. Plan to use in-line attenuators and DAC offset
  - BCMs: CREX saw nominal signal levels of ~1.3V from the analog BCM receivers
  - Cavity BPMs: CREX saw <2V on the Q signals and a range of +/-1V on the position signals; Plan to use in-line attenuators and DAC offset
  - Raster pickoff: CREX saw triangle wave with <2V amplitude; Plan to use in-line attenuators and DAC offset

Rack space estimate for DAQ for 40U (70inch) racks

- Integration mode: 71U in Hall, 31U in INJ
  - Integrators, 1U rackmount units, assume +1U for airflow
    - INJ: 6 modules → 12U: 0.3 rack
    - Hall A: 26 modules → 52U: 1.3 racks
  - VME/VXS: 11U height, front to back airflow
    - Trigger distribution in Hall
    - Trigger supervisor in INJ
  - NIM crate: 7U +1U
    - One each in Hall and INJ
  - **Don't have space needs for HVMAPS or digital BCM receivers yet**
  - **Doesn't include integrator power supplies, or the HV and LV supplies**
- Counting mode: 44U (+16U) in SBS bunker, 22U in downstream doghouses
  - Three VXS crates: 11U each, front to back airflow → 44U
  - Two VME crates in two "doghouses": 11U each, front to back airflow
  - Two NIM crates for amps in SBS bunker?: 7U+1U for airflow each → 16U
- SBS bunker: 3+0.4? racks; Doghouses: 0.3+0.3 racks; INJ: 0.8+ rack

Dual-mode amplifier design from Mainz



This is the circuit diagram of the dual-mode amplifier designed by Mainz.

The counting mode amp performance was comparable (or better) than a commercial NIM amp.

Michael expects to include the counting mode amp in the next version of the base design

Would then check performance with ~100m cable

Jefferson Lab

CODA readout/control of custom modules

Integrating ADC modules, HVMAPS FPGA readout, and the digital BCMs should all act as independent CODA readout controllers with internal Trigger Interfaces

- Trigger interface module functionality is being designed into the firmware for the integrating ADC, and TI connection will be made through QSFP on the main board

- The HVMAPS readout is expected to use a similar FPGA/SOM as the integrating ADCs so will use the TI firmware development for the integrating ADCs. The QSFP connection likely through an FMC adapter board which has been designed by JLab

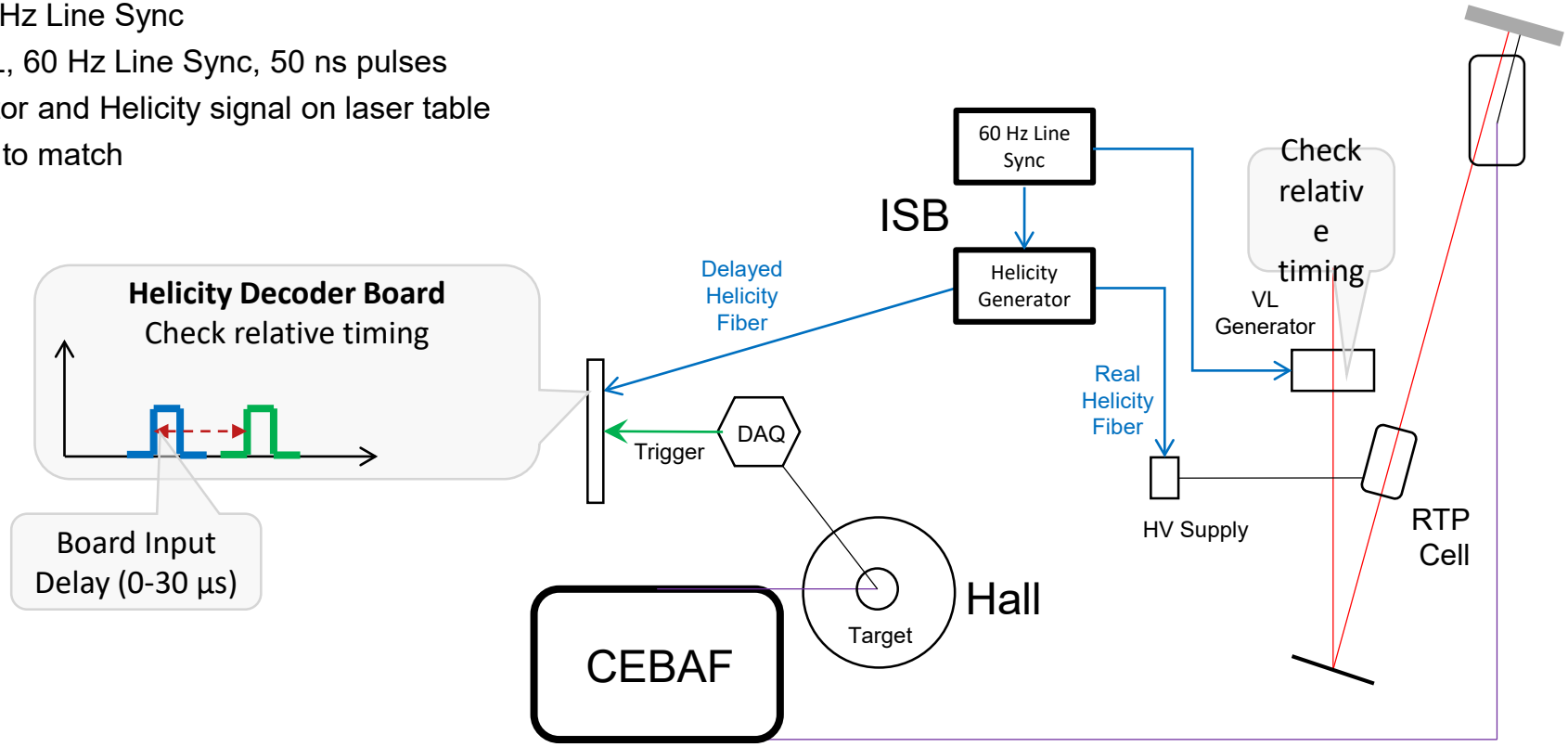
- The digital BCM uses a different FPGA board and will not have a free FMC. LBNL is developing a special adapter board (similar to the JLab FMC TI) for the QSFP connection, and would incorporate the TI firmware in the design

Effect of gate time mismatch

- If an integrator gate is not properly aligned with the spin flip then the measured asymmetry will be deceased by a percentage of about twice the fractional misalignment
  - Electron beam transit through the machine is ~20μs
  - Alignment within 200ns out of 500μs (0.04% misalignment) would bound this effect ~0.08% decrease in the asymmetry
  - If the detector and beam current monitor integrals are not aligned with respect to each other, then a false asymmetry is introduced which is equal to the charge asymmetry times twice the timing mismatch percentage. This would appear as a detector non-linearity
- Using a narrow beam pulse at 60 Hz (tune mode) and the diagnostic waveforms from the detector and beam current monitor modules, we expect to be able to adjust the relative gate timing to 2 or 3 of the 15 MHz samples, which would be about 0.1-0.2μs

Setting Board Programmable Delays

- With 10 μs T_Settle time, travel time from photocathode to Hall target becomes relevant. At 5th pass, travel time is ~21 μs. Helicity signal propagation to the hall is ~2.5 μs.
- How to set input time delays:
  - Helicity Board: 60 Hz Line Sync
  - Electron Beam: VL, 60 Hz Line Sync, 50 ns pulses
  - Check VL Generator and Helicity signal on laser table
  - Adjust gate timing to match



Slide courtesy of R. Suleiman

Integration mode data rate calculation

- Production mode:
  - Read out data for each helicity window separated into 4 blocks (4 data units)
  - Each data unit consists of 4 items:
    - The sum, sum of squares, minimum, maximum, and number of the collected samples
    - (calculating these is done in the FPGA) → 4+8+4+4+2 = 22 bytes
  - At 15 Msps ~7000 ADC samples per window from which to calculate these
  - 4 data units x 22 = 88 bytes / channel / window
  - Add 8 bytes for one timestamp per helicity window -> 96 bytes / channel /window
  - With 16 channels per board with one readout link that's about ~ 2kB / helicity window per board or ~4 MB / sec per board
  - Then 32 modules gives ~130 MB/s

- For diagnostic purposes and during tracking readout every ADC sample for selected channels at ~34 MB/sec/channel
  - One uses is to check gate timing with tune mode beam; helicity windows can be prescaled

Counting Mode Triggering

- GEMs/trigger scintillators inserted
- reduced beam current (≈100 pA) [100pA → Moller rate is ~30kHz/septant]
- use of thin ^{12}C targets, and the lH_2 target
- some measurements with "sieve" collimator to select scattering angles

1. Primary Counting-Mode Trigger
   - Trigger: "OR" of $i = 1,7$ of $[TS^i_{up} \cdot TS^i_{down}]$
2. Quartz-triggered mode
   - Triggers: possibility to select:
     a) OR of all thin quartz detectors in a given ring
     b) OR of all ShowerMax detectors
3. Pion-triggered modes
   - Triggers: possibility to select from:
     a) OR of all 7 pion detectors (cosmics, setup)
     b) OR of the two $(i = 1,2)$ ANDs: $[\pi TS^i_{up} \cdot \pi TS^i_{down}]$ (main pion dilution measurement)
     c) [OR of all 7 pion detectors] · [OR of all $TS^i_{up} \cdot TS^i_{down}$] (rate symmetry of pions; πTS efficiency; enhance pion signal)

Counting DAQ rates & data size

- FADC trigger window range: 100ns (25 samples)
- GEM samples: 3 25-ns samples

- Total Moller rate: 135 GHz@65 uA → ~300 MHz/sector/uA
  - At 100nA, ~30MHz/sector, 3 hits/sector/100ns
    - Likely use a pulser trigger at this beam current and find scint. hits in analysis
  - At 100pA, ~30kHz/sector

- FADC raw mode data rate at 7kHz: 150 MB/s
  - 336 FADC channels * (25 samples * 2 bytes/sample + 4 bytes for channel) → 127 MB/s
  - Estimate 8 particles with 5 detectors hit (2 scint, 1 quartz, 1 showermax, & 1 pion) in each sector per trigger; pulse parameter data would give ~23 MB/s

GEM data rate estimate

- 30 GEM modules (4 in each septant, plus 1 in each of two pion detectors)
- 1280 channels per module
- Readout: 300 APVs to 20 MPDs
- With 3 samples/chan & 16 bits/sample
  → 1.84Mb/event without data suppression
- At 7kHz maximum APV rate with 3 samples
  → 12.9Gb/s; 0.645 Gb/s from each MPD
- Occupancy (per 75ns window) expected due to Møllers at 100nA: ~2%
  - 3 e-e scatters per sector in 100 ns
  - 8 strips hit/module/track
  - 24 strips hit per event out of 1280
- With zero suppression at the VTP, and a 5% occupancy at 7kHz
  → 80.6 MB/s to disk

Online Analysis

- Needed Tasks
  1. Helicity correlated (HC) feedback
     - Feedback cycle likely 10 s
  2. Monitor of data quality
     - Some issues only appear at high statistics, needing hours or days
     - Requires correction for HC beam properties
  3. Monitor of transverse beam polarization
     - Requires corrections for HC beam properties
     - Requires accumulating multiple hours of data
- Hardware needs
  - One workstation for helicity-correlated feedback
  - 10 workstations for full analysis to support #2 and #3 (~50 concurrent jobs)
  - 100 TB fileserver provides space for several days of raw data and analysis results (raw data rate is 450 GB/hr, outputs are similar in size)

Data reduction and visualization

- The total raw data volume will be at the petabyte scale
- Creating ROOT TTrees of all elements would also result in petabyte scale output files
- Several parallel data reduction choices
  - Average yields and asymmetries for all data elements over short period (~1 minute?) and store in a database
  - Generate ROOT TTrees for only the key elements for all helicity patterns
  - Keep the full ROOT TTrees for a small subset of data files
- Anticipate needing a few hundred TB of disk space to work with the output files
- We will also need robust ways to monitor system performance and present output results to analysis workers