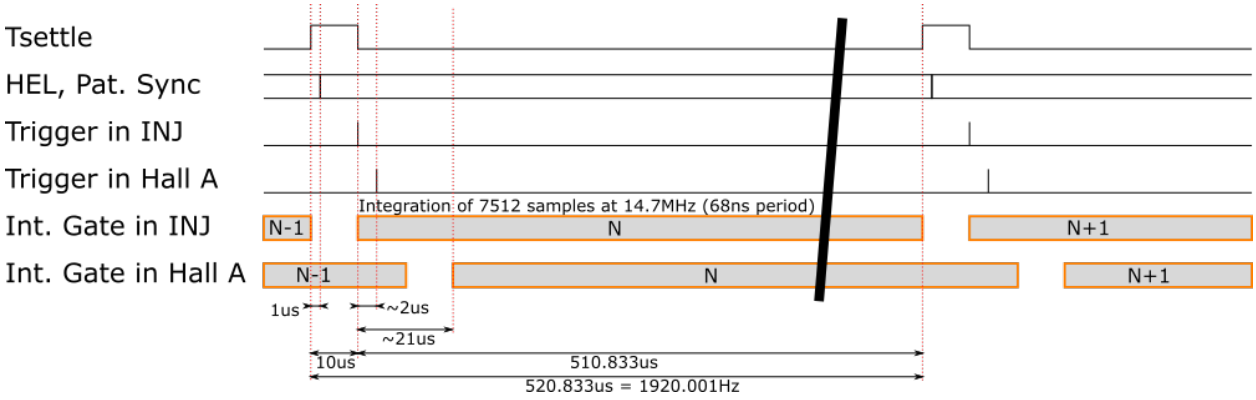
Integration mode timing diagram and notes

P. King; Draft, 8 September 2021



The helicity events are expected to be run at about 1920 Hz. A period of 520.833 us would permit the planned 10 us T_settle and a 510.833 us stable helicity state.

The helicity and pattern sync transitions are expected to be 1 us after the beginning of the Tsettle period.

We plan to form the trigger from the start of the T_stable period in the injector; the signal propagation from the TI-master in the ISB to the Hall A TI-bridge module is roughly 2 us.

The sampling clock in the integrating ADC is expected to be 14.7 MHz (250 MHz / 17 → 68 ns period), so we would want to accumulate 7512 samples to match the T_stable period (7512*68 ns==510. 816 us). The total of 7512 samples will be divided into 4 subblocks of 1878 samples each.

The electron beam propagation for 5-pass beam is about 21 us, so the integration gate in the hall would need to begin 21 us later than the gate in the hall. Also given the trigger propagation, the integration gate would begin ~19 us after the trigger arrives in the hall.

If we trigger a helicity event and wait for the data to be ready for that integration gate, then the system busy for event N would begin at the INJ trigger and lasts until the end of the hall integration gate, then the system will be busy when the next trigger would arrive at the INJ TI-master. Or maybe we don't need to have a system busy that lasts for the integration window?

Each module produces about 2 kB per helicity window. If a module could transmit its data at 1 Gbit/s, the data transfer for one event would be 16 us. With 32 modules sharing 10 Gbit/s, the data transfer for one event would be ~100 us.