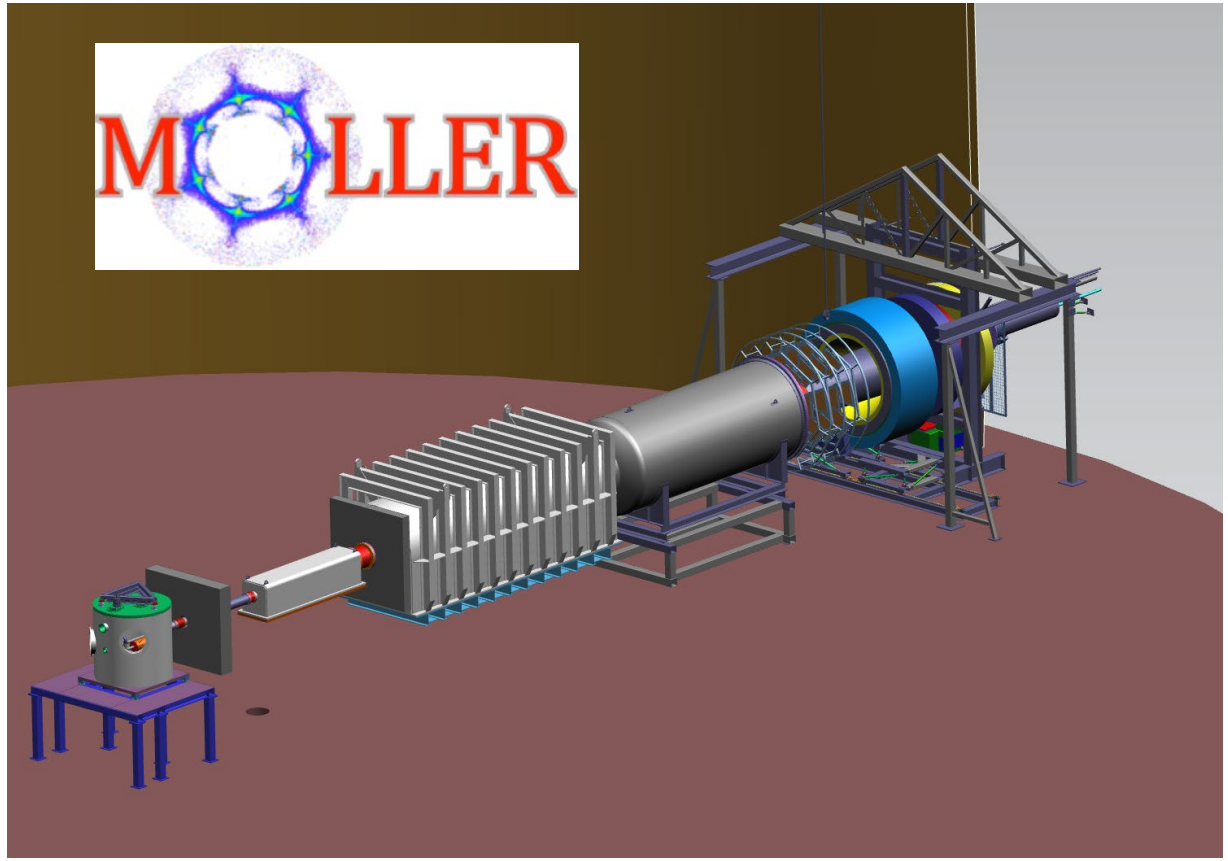
DAQ update

Integration and counting mode DAQ planning for MOLLER

MOLLER Collaboration meeting, 15-17 June 2021



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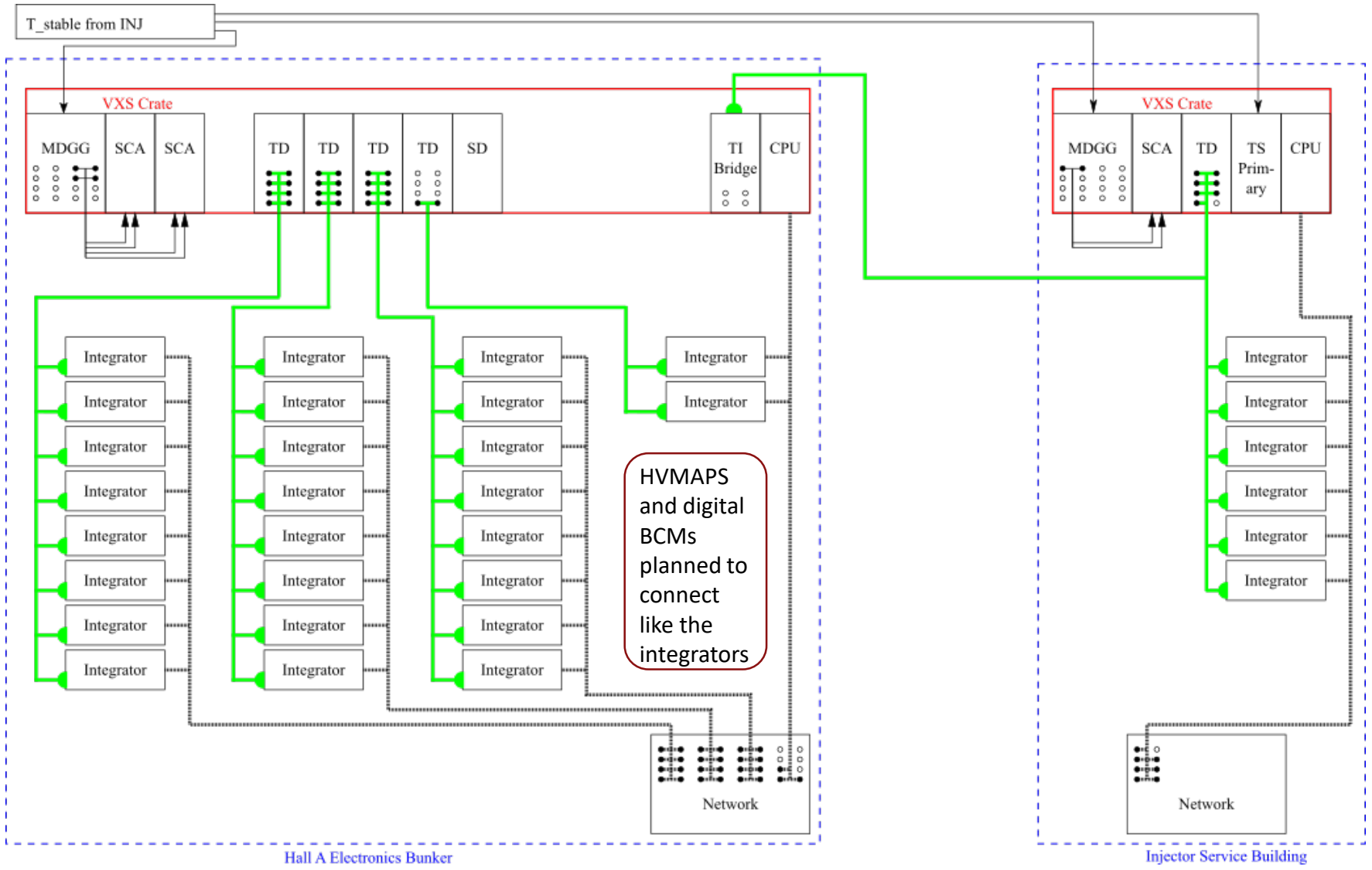
JSA

DAQ development contributors

- Integration mode
  - D. Bishop, B. Shaw; TRIUMF
  - B. Blaikie, M. Gericke, J. Pan; University of Manitoba
  - W. Gu; JLab
- Counting mode
  - D. Armstrong; William and Mary
  - C. Ghosh, H. Liu; University of Massachusetts, Amherst
- Digital BCM
  - J. Arrington, Y. Kolomensky, S. Li, Y. Mei, E. Sichtermann; LBNL
  - W. Gu; JLab

- All three teams involve
  - R. Michaels, B. Moffit; JLab
  - P. King; Ohio University

Integration DAQ layout



Helicity trigger is formed in ISB, so that INJ gate is formed promptly

Gate timing adjusted per module to account for ~20µs electron transit or other signal latencies; need ~0.1µs resolution

TI Bridge feeds SD/TDs to distribute gates/triggers

TI to Integrator connection use one QSFP connection

10Gb/s network on QSFP connections

Integration mode channels

- Detector array (266 total)
  - 224 Main detectors, 28 shower-max detectors, 14 pion detectors
- SAMs, LAMs, and beamline (233 channels)
  - SAMs: 8
  - LAMs and diffuse background monitors: 28
  - Injector beamline: 96
  - Transport line and Hall beamline: 101 (PREX/CREX used 64; my count so far ~77 ch.)
- Scanner (13 channels)
  - X/Y scanner: 2 PMTs + 2 position voltages
  - Linear scanners: 4 PMTs + 4 position voltages
  - Reference voltage for positions
- Total: 512 channels → 32 16-channel modules

- Not fully included in design: HVMAPS; Digital BCM

CODA readout/control of custom modules

Integrating ADC modules, HVMAPS FPGA readout, and the digital BCMs should all act as independent CODA readout controllers with internal Trigger Interfaces

- Trigger interface module functionality is being designed into the firmware for the integrating ADC, and TI connection will be made through QSFP on the main board

- The HVMAPS readout is expected to use the same FPGA/SOM as the integrating ADCs so will use the TI firmware development for the integrating ADCs. The QSFP connection likely through an FMC adapter board which has been designed by JLab

- The digital BCM uses a different FPGA board and will not have a free FMC. LBNL is developing a special adapter board (similar to the JLab FMC TI) for the QSFP connection, and would incorporate the TI firmware in the design

Effect of gate time mismatch

- If an integrator gate is not properly aligned with the spin flip then the measured asymmetry will be deceased by a percentage of about twice the fractional misalignment
  - Electron beam transit through the machine is ~20μs
  - Alignment within 200ns out of 500μs (0.04% misalignment) would bound this effect ~0.08% decrease in the asymmetry
  - If the detector and beam current monitor integrals are not aligned with respect to each other, then a false asymmetry is introduced which is equal to the charge asymmetry times twice the timing mismatch percentage. This would appear as a detector non-linearity
- Using a narrow beam pulse at 60 Hz (tune mode) and the diagnostic waveforms from the detector and beam current monitor modules, we expect to be able to adjust the relative gate timing to 2 or 3 of the 15 MHz samples, which would be about 0.1-0.2μs

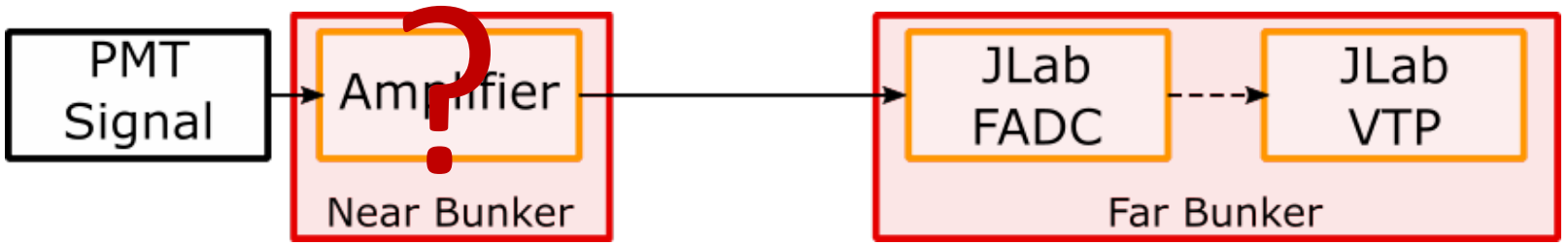
Signal levels in integration mode

- The integrating ADC module base design uses a differential input with both pins accepting a -2V to +2V range, allowing a -4V to +4V signal range

- PMT signals: the transimpedence preamplifiers are designed to match the ADC input.

- Beam monitor signals from JLab instrumentation are available as single-ended signals. By shorting one of the two pins on an ADC input, it will take a single-ended input with signal range of -4V to +4V. Need cable adaptation as well.
  - Stripline BPMs: The S&H cards output a nominal 3V signal (potentially chosen in either polarity), but the signal can go to 5V. Need to attenuate the signals?
  - BCMs: CREX saw nominal signal levels of ~1.3V from the analog BCM receivers
  - Cavity BPMs: CREX saw <2V on the Q signals and a range of +/-1V on the position signals
  - Raster pickoff: CREX saw triangle wave with <2V amplitude; the raster is being reworked & currents will be higher → What range do we expect for raster pickoff?

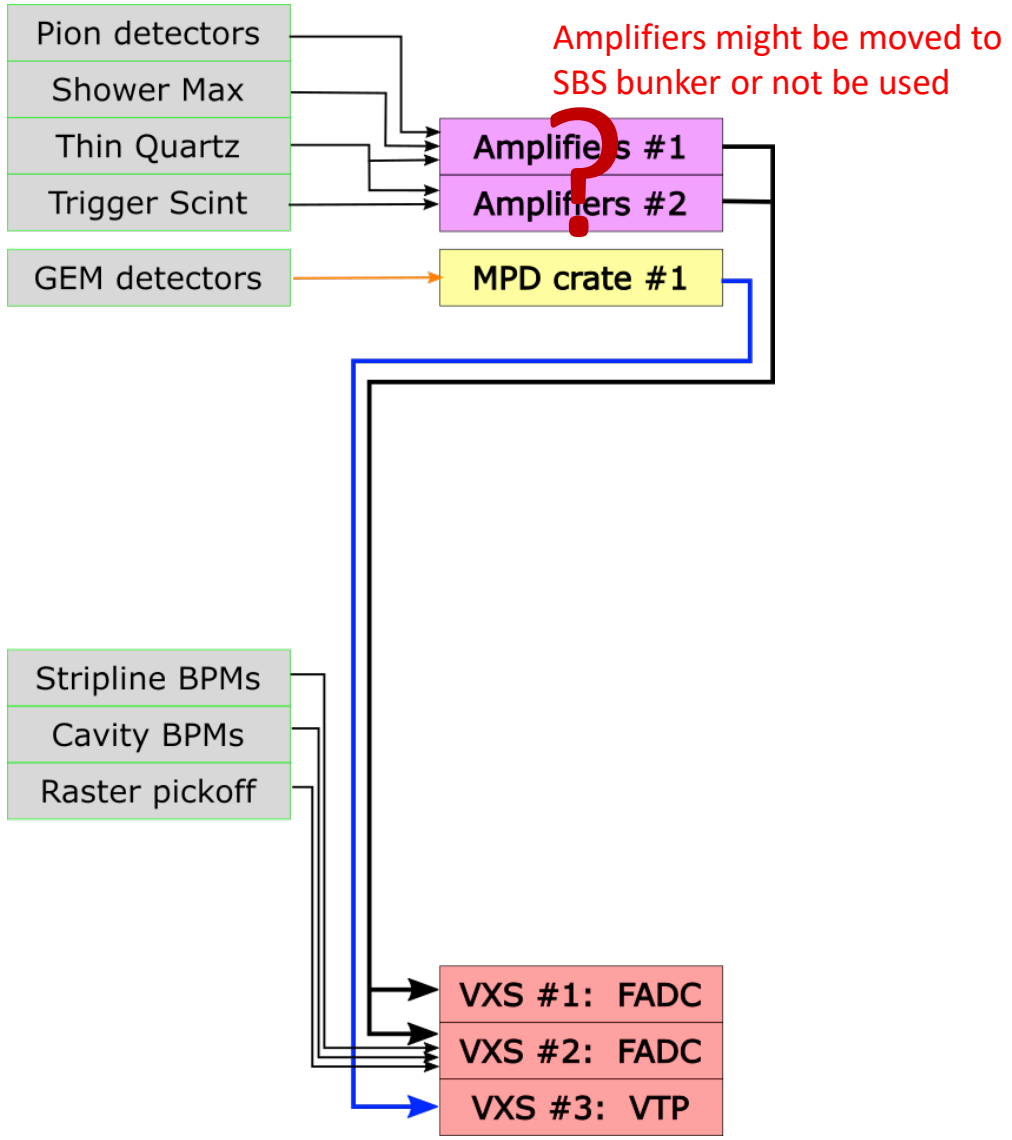
Counting Mode Data Acquisition and Trigger



- Voltage and timing data: 304 ch. (19 FADC)
  - Detector array PMTs: 266 total; 224 thin quartz, 28 shower-max, 14 pion detectors
  - Trigger scintillators: 18; 2 each for 7 GEM sectors & 2 pion sectors
  - Scanner PMTs: 6; 2 in X/Y scanner and 1 each in 4 linear scanners
  - Alternate trigger signals: 14; SAM- or LAM- signals? Diffuse background PMTs? Halo PMTs?
- Voltage data only: 23 ch. (2 FADC)
  - Beamline: Two cavity triplets and two stripline BPMs: 14 ch.
  - Raster readbacks: 2 ch.
  - Scanner position: 7; 2 for X/Y, 4 for linear scanners, 1 voltage reference
- GEM readout: APV25→MPD→VTP

Counting mode cable and crate layout

- PMT signals go through 600” RG58 cables to NIM amplifiers in the small bunker, then 320’ RG58 cables to main electronics hut patch panel
- From main electronics hut patch panel, 600” RG58 cables connect to the FADCs
- Beam monitor signals run on RG58 cables (length TBD) from the standard Hall A electronics racks to FADCs
- GEM signals from 30 modules (28 tracking, 2 pion) go to the 20 MPDs (2 crates of 10?) in the small bunker, then to a VTP in the main electronics hut



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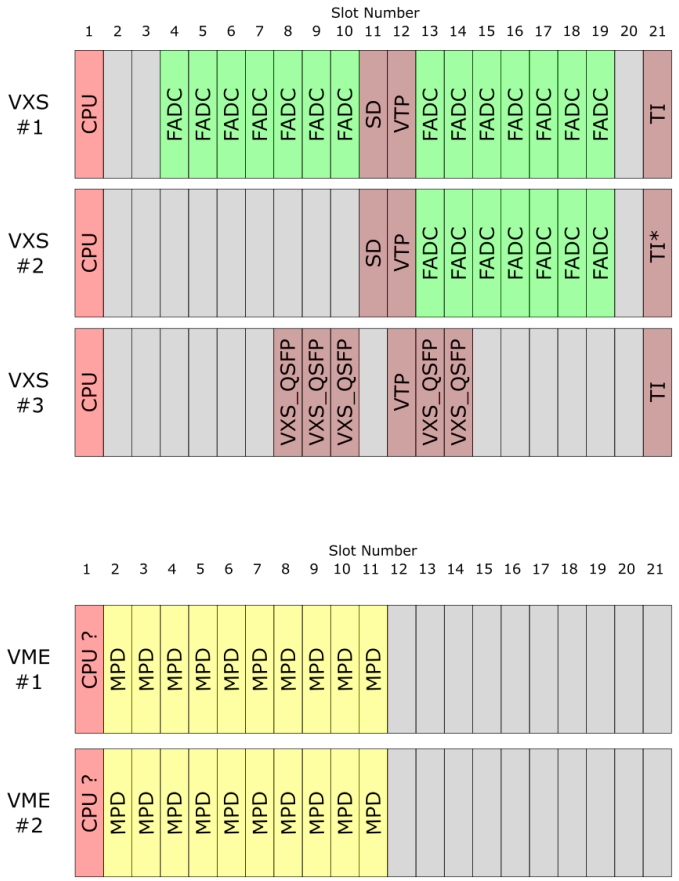
Counting mode crate layout without fast amplifiers



- VXS #1: Rings 1 – 4, Ring 5 & 6
- VXS #2: Shower max, Pion detectors, Trigger scintillators, Scanner, Alternates; Voltage-only signals

- VXS #3: 20 MPDs readout through VTP
  - One crate of 10 MPDs in each of two minibunkers?

Trigger formation

- Trigger thresholds defined in FADCs
- FADC trigger information sent to VTP for processing
- VTPs in VXS #1 & #2 send triggers to TI-master

Signal levels in counting mode

- The FADC can have a negative going range of 0V to -2V (or similar for positive)
- PMT signals: Signals should be within the input range
- Beam monitors
  - Stripline BPMs: The S&H cards output a nominal 3V signal (potentially chosen in either polarity), but the signal can go to 5V. Need to attenuate the signals
  - BCMs: CREX saw nominal signal levels of ~1.3V from the analog BCM receivers
  - Cavity BPMs: CREX saw <2V on the Q signals and a range of +/-1V on the position signals; need baseline shift for positions?
  - Raster pickoff: CREX saw triangle wave with <2V amplitude; the raster is being reworked & currents will be higher → What range do we expect for raster pickoff? Need baseline shift and may need attenuation

Rack space estimate for DAQ for 40U (70inch) racks

- Integration mode: 71U in Hall, 31U in INJ
  - Integrators, 1U rackmount units, assume +1U for airflow
    - INJ: 6 modules → 12U: 0.3 rack
    - Hall A: 26 modules → 52U: 1.3 racks
  - VME/VXS: 11U height, front to back airflow
    - Trigger distribution in Hall
    - Trigger supervisor in INJ
  - NIM crate: 7U +1U
    - One each in Hall and INJ
  - **Don't have space needs for HVMAPS or digital BCM receivers yet**
  - **Doesn't include integrator power supplies, or the HV and LV supplies**
- Counting mode: 44U in SBS bunker, 22U (+16U) in downstream bunkers
  - Three VXS crates: 11U each, front to back airflow → 44U
  - Two VME crates in two downstream bunkers: 11U each, front to back airflow
  - Two NIM crates in downstream bunker or SBS bunker?: 7U+1U for airflow each → 16U
- SBS bunker: 3+ racks; Downstream bunkers: 0.4?+0.3+0.3 racks; INJ: 0.8+ rack

Milestones & Plans

- Orders go out for test stand instrumentation modules: 21 July 2021
- Verification of test system: Oct/Nov 2021 – Feb/Apr 2022
- 90% design preparation and review: Apr 2022 – May 2022

- Support of PQB studies
  - For the summer, we are using INJ crate only, running CODA 2.6.2
  - To run with hall beamline devices, we likely need to upgrade to CODA 3.10, with a new CPU in INJ crate
    - There is also concern about isolating parity DAQ network traffic from SBS traffic due to very high data rates in SBS

- For the 90% review (or sooner), need to have the plan for certifying the electronics modules with the new guidance from Electrical Safety committee

Paul King

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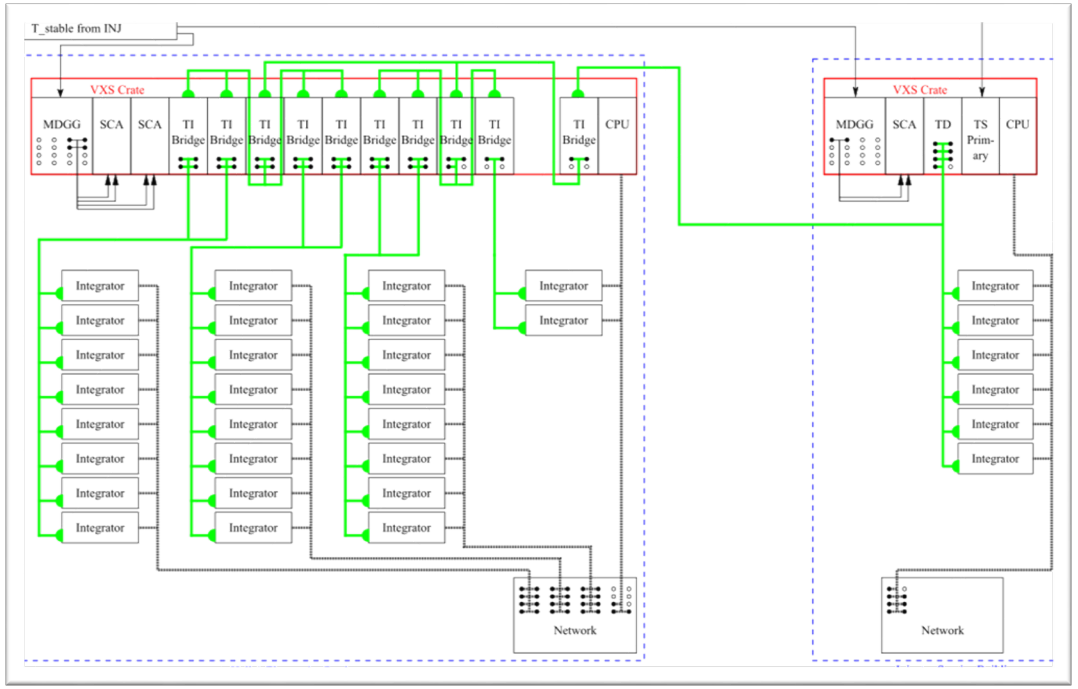
Summary

- Integrating and counting DAQ working groups are continuing to refine the designs and prepare the design and interface documents
  - Reaching out to other groups to check channel counts → Ask me if **your** favorite channels have been counted!
- Digital BCM and HVMAPS plans are continuing to develop, but less advanced
- Test stands and experience from SBS will help us get ready for 90% review next spring

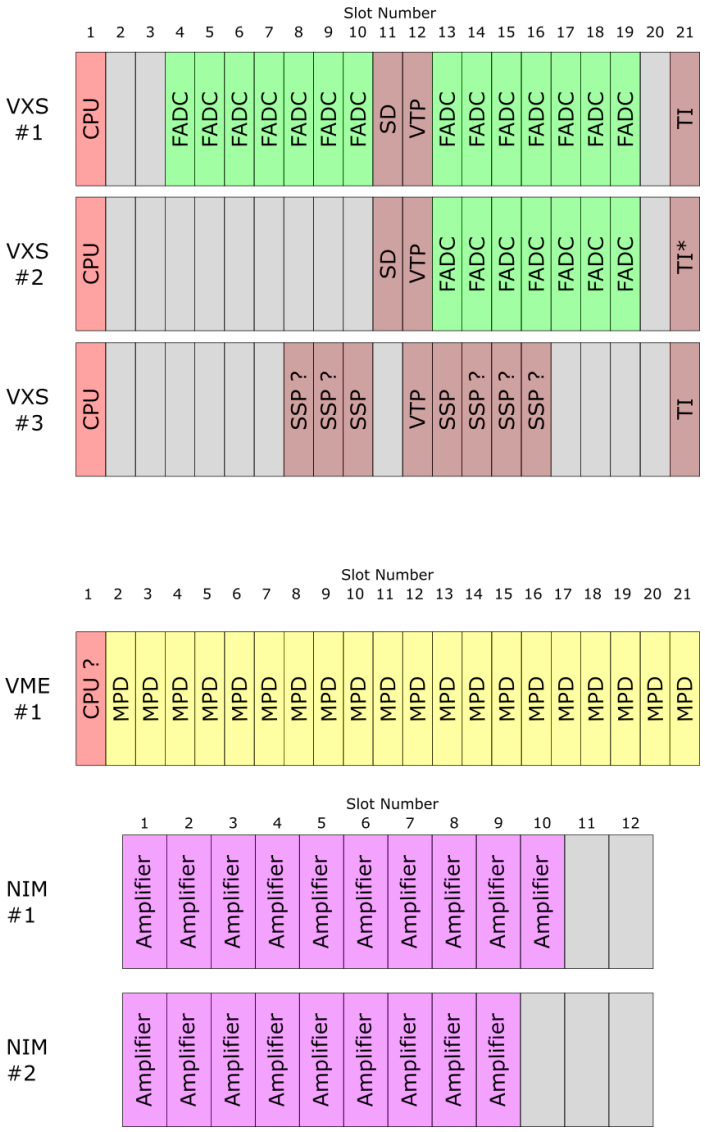


Counting Mode Triggering

- GEMs/trigger scintillators inserted
- reduced beam current (≈100 pA) [100pA → Moller rate is ~30kHz/septant]
- use of thin ^{12}C targets, and the lH_2 target
- some measurements with "sieve" collimator to select scattering angles

1. Primary Counting-Mode Trigger
   - Trigger: "OR" of $i = 1,7$ of $[TS^i_{up} \cdot TS^i_{down}]$
2. Quartz-triggered mode
   - Triggers: possibility to select:
     a) OR of all thin quartz detectors in a given ring
     b) OR of all ShowerMax detectors
3. Pion-triggered modes
   - Triggers: possibility to select from:
     a) OR of all 7 pion detectors (cosmics, setup)
     b) OR of the two $(i = 1,2)$ ANDs: $[\pi TS^i_{up} \cdot \pi TS^i_{down}]$ (main pion dilution measurement)
     c) [OR of all 7 pion detectors] · [OR of all $TS^i_{up} \cdot TS^i_{down}$] (rate symmetry of pions; πTS efficiency; enhance pion signal)

Counting mode crate layout (with amplifiers)



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Integration mode data rate calculation

- Production mode:
  - Read out data for each helicity window separated into 4 blocks (4 data units)
  - Each data unit consists of 4 items:
    - The sum, sum of squares, minimum, maximum, and number of the collected samples
    - (calculating these is done in the FPGA) → 4+8+4+4+2 = 22 bytes
  - At 15 Msps ~7000 ADC samples per window from which to calculate these
  - 4 data units x 22 = 88 bytes / channel / window
  - Add 8 bytes for one timestamp per helicity window -> 96 bytes / channel /window
  - With 16 channels per board with one readout link that's about ~ 2kB / helicity window per board or ~4 MB / sec per board
  - Then 32 modules gives ~130 MB/s

- For diagnostic purposes and during tracking readout every ADC sample for selected channels at ~34 MB/sec/channel
  - One uses is to check gate timing with tune mode beam; helicity windows can be prescaled

Counting DAQ rates & data size

- FADC trigger window range: 100ns (25 samples)
- GEM samples: 3 25-ns samples

- Total Moller rate: 135 GHz@65 uA → ~300 MHz/sector/uA
  - At 100nA, ~30MHz/sector, 3 hits/sector/100ns
    - Likely use a pulser trigger at this beam current and find scint. hits in analysis
  - At 100pA, ~30kHz/sector

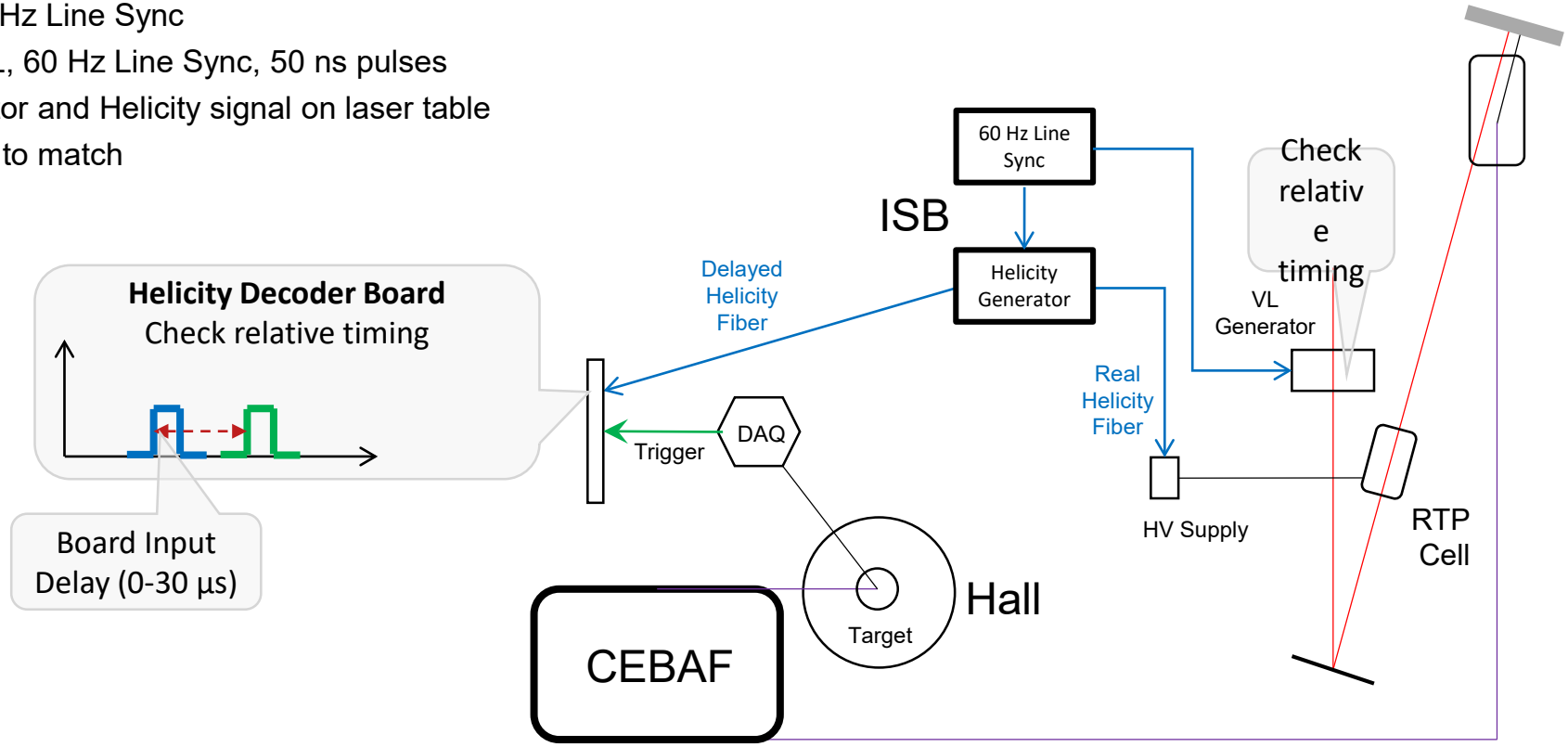
- FADC raw mode data rate at 7kHz: 150 MB/s
  - 336 FADC channels * (25 samples * 2 bytes/sample + 4 bytes for channel) → 127 MB/s
  - Estimate 8 particles with 5 detectors hit (2 scint, 1 quartz, 1 showermax, & 1 pion) in each sector per trigger; pulse parameter data would give ~23 MB/s

GEM data rate estimate

- 30 GEM modules (4 in each septant, plus 1 in each of two pion detectors)
- 1280 channels per module
- Readout: 300 APVs to 20 MPDs
- With 3 samples/chan & 16 bits/sample
  → 1.84Mb/event without data suppression
- At 7kHz maximum APV rate with 3 samples
  → 12.9Gb/s; 0.645 Gb/s from each MPD
- Occupancy (per 75ns window) expected due to Møllers at 100nA: ~2%
  - 3 e-e scatters per sector in 100 ns
  - 8 strips hit/module/track
  - 24 strips hit per event out of 1280
- With zero suppression at the VTP, and a 5% occupancy at 7kHz
  → 80.6 MB/s to disk

Setting Board Programmable Delays

- With 10 μs T_Settle time, travel time from photocathode to Hall target becomes relevant. At 5th pass, travel time is ~21 μs. Helicity signal propagation to the hall is ~2.5 μs.
- How to set input time delays:
  - Helicity Board: 60 Hz Line Sync
  - Electron Beam: VL, 60 Hz Line Sync, 50 ns pulses
  - Check VL Generator and Helicity signal on laser table
  - Adjust gate timing to match



Slide courtesy of R. Suleiman

Online Analysis

- Needed Tasks
  1. Helicity correlated (HC) feedback
     - Feedback cycle likely 10 s
  2. Monitor of data quality
     - Some issues only appear at high statistics, needing hours or days
     - Requires correction for HC beam properties
  3. Monitor of transverse beam polarization
     - Requires corrections for HC beam properties
     - Requires accumulating multiple hours of data
- Hardware needs
  - One workstation for helicity-correlated feedback
  - 10 workstations for full analysis to support #2 and #3 (~50 concurrent jobs)
  - 100 TB fileserver provides space for several days of raw data and analysis results (raw data rate is 450 GB/hr, outputs are similar in size)

Data reduction and visualization

- The total raw data volume will be at the petabyte scale
- Creating ROOT TTrees of all elements would also result in petabyte scale output files
- Several parallel data reduction choices
  - Average yields and asymmetries for all data elements over short period (~1 minute?) and store in a database
  - Generate ROOT TTrees for only the key elements for all helicity patterns
  - Keep the full ROOT TTrees for a small subset of data files
- Anticipate needing a few hundred TB of disk space to work with the output files
- We will also need robust ways to monitor system performance and present output results to analysis workers